VDU-K MANUAL

Interak

Document Ref: VDUK-1/3

Issue: 1.3

Date: October 1982
(Reprinted May 1983
and May 1984)

VDU-K INTERAK 1 VDU INTERFACE

USER MANUAL - ISSUE 3

Manual Price £2.50

ISSUE 2 MANUAL VDU-K SINGLE CARD VDU

PREFACE

This is a card produced especially for the Interak 1 computer.

It is an 'Applications' card, in that it is designed to permit low cost applications of computer displays using a standard domestic T.V. receiver, whilst still retaining high quality.

Many diverse applications are possible due to the fact that the character set used is held in EPROM and thus may be specified to suit the particular application.

A very low dot clock (6 MHz) has been used, which is the secret of obtaining a high quality display on an ordinary T.V. receiver, and various design refinements have been incorporated (e.g. generation of proper T.V. sync. pulse waveforms, provision of choice of interlaced/non-interlaced display) to ensure that the card can be used with confidence in its chosen application.

The outstanding feature is the avoidance of "snow", (the interference effect which is often seen in low-cost designs when the microprocessor accesses the screen during the display time). In consequence this board is ideally suited for very fast animated displays.

The screen format employs characters of a good size which are approximately square, and so it is very easy to make a display which aesthetically is very pleasing .

One application for which the card is less suited is that in the "professional" and "business" worlds, in those applications where one user wishes to view large quantities of alphanumeric data or text. In such an application the ability to produce fast animations viewable by a group of people is less important; there is a fair amount of truth in the statement that it is only necessary to fill a screen with text at a rate which is faster than it can be read and high speed of access is only a luxury.

It is anticipated that for word-processing etc. applications some alternative to the VDU-K will become available in the Interak range, but as serious word-processing etc. often goes hand in hand with the use of relatively expensive floppy disks and VDU terminals, it is likely that there will always be a place for the VDU-K in a low-cost system. (Note however that the "Interaktion" Users Group has details of a fairly simple modification to permit 64 characters on the VDU-K, although this is at the expense of the "no snow" feature. See User Group Newsletter Number 2, March 1983.)

ISSUE 2 MANUAL VDU-K SINGLE CARD VDU

CONTENTS

(Total no. of pages Issue 2: 90)

ERRATUM

October 1982: Issue 1.1

May 1983: Issue 1.2

September 1983: Issue 1.2 reprinted

May 1984: Issue 1.3

In this manual reference is made to the use of a switch "S3" which is intended to provide a "Reverse All" option. In general this switch will work only with TV receivers, giving a blank screen on a video monitor. A full explanation is to be given in the "Interaktion" Newsletter Issues 3 and 4, but the result is that this option cannot always be used.

ADDENDUM

May 1984: The kits prepared for this card now include new components described as "JLinks" in the relevant price lists. These are push-fit shorting links which connect two adjacent posts on the 0.1" pitch pin assemblies. This is more convenient than using the other recommended connection method, wire wrapping. If JLinks are supplied use them wherever possible in preference to wire wrapping and disregard any part of this manual which suggests wire wrapped connections between adjacent pins.

MOS ETC. DEVICES.

Precautionary Notice

Some of the Integrated Circuits used on this card are supplied packed in special anti-static packing (tubes, foil, or foam), and have a warning notice affixed to the packing.

Do not be alarmed, experience shows that damage due to mis-handling very rarely happens.

The damage is due to static electric charges, being transferred from an object or person through the leads of the integrated circuit to the tiny chip inside. Only some types of IC are vulnerable, e.g. MOS or CMOS types, and some of the latest shallow diffusion high-speed bipolar types.

The initials MOS stand for "Metal-Oxide-Semiconductor". The oxide is, for example silicon dioxide - an excellent insulator, which insulates the metal from the silicon.

However the scale of IC chip manufacture is so small that the layer of oxide is easily damaged by excessive static charges which "punch through" the insulating layer.

Sometimes the damage is not immediately noticed (which might explain how some people disregard all precautions and appear to get away with it), but during the months and years which follow, metal "ions" can migrate through the hole and failure can eventually result.

We would liken the risk of causing this damage to the risk of getting caught "speeding" in a motor car. Of course there are people who disregard all speed limits and never get caught, just as there are people who disregard handling precautions with no adverse effects. But do remember, every so often you meet someone who has been disqualified from driving due to speeding, so do not let him handle your ICs!

The full set of handling precautions is given on the next page; as mentioned, not everybody follows them all to the letter, but at least you cannot say you haven't been warned!

HANDLING PRECAUTIONS TO AVOID DAMAGE TO MOS INTEGRATED CIRCUITS BY STATIC DISCHARGE

Before unwinding any wire shorting together the pins of the ICs, or removing the ICs from their protecting metal or anti-static carrier tube, container, or anti-static foam, please read the following precautions:

1. Never use an isolated bit ("low leakage") soldering-iron to work on a circuit with the ICs in place. The bit should be earthed. If in any doubt, earth it by clipping on a small crocodile clip connected to earth. Similarly, all test equipment should be earthed before it is connected to a finished circuit.

2. Work on an earthed metal plate about a few feet square, (e.g. a stainless steel kitchen sink, or cooking foil), as a work-bench, when the time comes to install the ICs.

3. Keep all your tools on this earthed metal plate, and connect yourself to it, either by touching, or by using a piece of connecting wire formed as a wrist-strap. (Note: if you are using a wrist-strap, it is considered less hazardous to personal safety if the connection to earth is made via a 1 Megohm resistor.)

4. Before fitting the ICs, earth your circuit board, the IC sockets, and yourself; make sure that the power supply has been turned off and all electrolytic capacitors have been completely discharged.

5. Never leave unprotected ICs on a plastic or other non-conductive surface and never store them in ordinary white polystyrene without protection. (If a conductive tube or similar container is used, it is not possible for a damaging static potential to be built up inside such a container, nor could such a charge normally be introduced to the ICs from outside.)

6. Damage is less likely in humid conditions than dry ones. Try to avoid nylon and similar clothing, seating and carpeting, when working with these chips.

7. Use some form of IC sockets if you possibly can, as once the devices have been soldered, any guarantee which existed becomes void. If it is essential to solder the ICs, the supply pins should be soldered first, in order that the internal protection circuits have the maximum chance to carry out their task.

VDU-K SINGLE CARD VDU GENERAL FEATURES

* International Size Card (4.5" x 8").
* 32 characters x 24 lines.
* Character cell 8 x 10 dots.
* Character set held in EPROM (1 or 2 2716 or 2532/2732).
* Up to 256 different characters available, or 128, + 128 repeats in reverse video.
* "No snow" operation - works with Z80A at 4MHz with no wait states.
* Uses 200ns RAMs e.g. type 2114L-200.
* Single card (replaces earlier VDU-A,B,G).
* Space on board for wide-bandwidth Modulator (for use with standard TV set).
* Low dot rate clock (6 MHz) ensures high quality display on standard TV set.
* Direct composite video output for TV Monitor.
* Plated-through holes, Epoxy-glass PCB.
* Green Solder Resist on "A" side, (sometimes "B" side also).
* Gold-plated edge connector on both A and B sides.
* 5V only operation.
* Sync. pulses include equalisation pulses.
* Line sync. maintained during frame sync. time.
* Interlaced/non-interlaced option switch selectable.
* Uses dedicated Z80A to generate sync. pulse timing.
* Quartz crystal for timing accuracy.
* ASCII high-bit invert or alternative character set.
* Optional switch for "invert all".
* Standard character generator includes upper/lower case, pixel characters, and line drawing characters.
* Lower case characters have decenders, where appropriate.
* Character cells adjoin for continuous coverage.
* Memory Mapped, may be addressed at any 1K boundary.
* ISBUS-A, INTERAK 1 bus compatible.
* KBUS-5, KBUS-12 compatible.
* Buffered where necessary to reduce bus loading to 1 "LS" load per line.
* No manufacturer's name appears on the card, thus ideal for OEM (original equipment manufacturer) use.

2.1 INTRODUCTION

The VDU-K provides a high-quality display on a standard 625-line TV set, via its on-board wide bandwidth UHF modulator, or if desired a composite video signal is independently available to drive a TV monitor. The user can choose to have either black characters on a white background, or white characters on a black background, according to his or her personal preference.

The VDU-K appears to the computer as 1K of RAM, starting at any chosen 1K boundary, selected by DIL switches. However in fact only the first 0.75K of the VDU RAM is displayable, and the last 0.25K is available to the user (this can be quite useful in a very small system which involves a VDU-K, as there is sometimes no need for a separate RAM card). It should be noted that it is not possible to run programs in the video RAM, the timing restrictions are such that it can only be used as read/write memory.

The 7-bit ASCII code is used as the basis for the character definition, for example a "41" (hexadecimal notation) written to the first location in the VDU RAM would result in a letter "A" being displayed in the top left-hand corner of the VDU screen, "42" would be "B", and so on. As the entire character generator set is held in EPROM, any desired sequence or font of characters can be programmed. The total screen displays as 256 dots across x 240 dots down, so for special applications graphics characters having an equivalent resolution of 61,440 dots per screen can be programmed into the EPROM character generator. Examples of special dedicated applications are chess pieces, and pipes and steam valves etc. to give a very inexpensive "mimic" diagram for process control and the like.

The standard 2716 EPROM pre-programmed character generator provides 128 characters including all of the printable ASCII characters, upper- and lower-case letters, with "descenders" where appropriate. A 5x7 matrix is used for the majority of the characters, and the matrix is placed within the 8x10 character cell so that these inverted video characters do not "fall out" of the cell, and thus remain very readable. The non-printing ASCII characters (carriage-return, line-feed and so on) make up the remainder of the standard 2716 character generator. Line-drawing and "pixel" characters (quarter character squares) are displayed for most of the non-printing codes, and there are a few graphics characters in the remaining space.

If the 7-bit ASCII code is presented to the VDU-K in a byte with the high bit set, the displayed character will appear in inverse video, i.e. black will be white, and vice versa, for that particular character. An alternative option is to let the high bit select a whole new character generator EPROM, containing a further 128 pre-programmed characters, making 256 in all. The extra characters are normally contained in a second 2716 EPROM, but the pair of EPROMs can be replaced if desired by a single type 2532 or 2732.

The second set of characters if used is called the "Applications" character set, as they will depend to what application the VDU-K is being put. For an amusement arcade type of game the Applications

EPROM could contain assorted space invaders and the like, whereas for a computer aided circuit design application the EPROM could contain transistor, resistor, logic gate etc. symbols.

Any of the dots in the 8x10 character cell can be programmed into the EPROM character generator, and adjacent cells touch on the screen, so that the character set designer has a fairly free hand.

No Snow

The outstanding feature of the VDU-K is that there are no restrictions placed on the timing of CPU reads and writes. A Z80A operating at 4 MHz can read from or write to a location on the screen at any time, without causing any disturbance ("snow") whatever on the display. "Wait" states are not required, and in fact are detrimental since they prolong the CPU access long enough to deprive the VDU of its correct data and so cause "snow" on the screen. The CPU can be operated at a lower speed, but the anti-snow feature of the VDU-K will not be so effective.

A television sync. waveform has to be fairly complex if it is to meet the required specification. For example there should be five half line equalising pulses at the beginning and end of each frame, and the line sync. should be kept going during the frame sync. time. It is very rare even for modern computers to comply with these latter requirements; most often they discontinue the line pulses during the frame sync. time, and hope that the good natured television set line timebase can regain line synchronisation in time to avoid spoiling the display. If you look at the top few lines of the television output of many computers you will see what a forlorn hope this is, as there is often visible "pulling" at the top of the display.

As a television set has a fairly short persistence phosphor, better results are often obtained by choosing a "non-interlaced" display, since this refreshes individual picture elements at a 50 Hz rate rather than the 25 Hz rate of a fully interlaced display. Particularly when viewed from a metre or less, there is much reduced flicker with a non-interlaced display. The VDU-K has an alterable link (or switch setting if a switch is fitted) so that the user can select whichever he prefers.

Unique Sync. Circuit

The necessary complication of the sync. waveform circuit has been satisfied in a unique manner on the VDU-K. Instead of the several LS TTL packages that would have been required to generate the proper "no compromises" interlaced/non-interlaced sync. timing, a dedicated Z80A has been used. Although no work has been carried out on this question, it is possible that it would be fairly easy to modify the control program to suit other TV standards, e.g. 525 lines instead of 625.

Because of the good number of internal registers in the Z80A, no external RAM is needed in this application, and it turns out that the use of the Z80A for sync. generation uses less space than the

alternative solutions, and as a bonus is cheaper.

Sensible Screen Format

The number of characters across the screen is limited by the bandwidth of the television receiver. The number chosen (32) was selected for several reasons: to be compatible with earlier systems (e.g. VDU-A,B,G), and to enable much of the software for the Sinclair ZX-81 (which uses the same format) to be converted easily by users. The number 32 is the round figure "20" in hexadecimal, which makes the task of handling fast motion on the screen (one of the main applications of a "no snow" VDU) much easier to program. With a fairly large character cell like this a sizeable character block results if adjacent cells are joined together. This makes games such as "Space Invaders" much more enjoyable than if they are played with very small, cramped characters. Also the good size character is very legible especially at a distance, for example if displaying announcements (e.g. airport announcements, betting shop results etc.) on a television set. The final benefit attached to the number of characters chosen is the fact that the character cell is near enough square. Apart from improving legibility of alphanumeric characters, this means that 45 degree lines plotted using the pixel characters are very close to the correct angle, and a circle is very close indeed to being circular. (Unless you are experienced with computers you will be quite surprised to find how many circles plotted even on quite expensive machines are not circular at all.)

Easy Construction

All of the components used are readily available, and the 27 integrated circuits used are all laid out the same way round, which makes the card very straightforward to construct and test. Wherever possible signal tracks which have to pass between the legs of ICs are taken on the A-side so that they can be inspected in case of trouble. (Less considerate designers take them on the B-side where any shorts will be hidden under the IC sockets!) Plated-through hole construction is provided, and a solder resist mask on the A-side, sometimes also on the B-side.

Although all of the signals are taken via the A-side of the edge connector (which is gold-plated) and a gold-plated edge connector is also provided on the B-side.

Contents of Kit

The kit of components, which is sold separately to the p.c.b. itself, includes 18 resistors, 1 SIL resistor pack, 1 variable resistor, 17 capacitors, 2 diodes, 1 transistor, 1 12.0 MHz crystal, 26 integrated circuits (including the standard character generator, and sync. pulse generator), 28 integrated circuit sockets (including sockets for the optional DIL switch and 2nd character generator), and some wiring pins. A 1" metal card front and some connectors and option switches are recommended but are not included in the kit to keep the basic cost down for those working to limited budgets. Also note that the wide

bandwidth modulator (Type UM1233 E36) should be purchased separately. It has not been included because an increasing number of users now have Video Monitors, and/or can salvage a modulator from a disused computer, e.g. ZX-80.

For the convenience of those users who may already have some of the parts required, all of the components are available separately. EPROMs already programmed with the timing program and a standard character generator set can be supplied at modest cost.

2.2 VDU-K CARD GENERAL DESCRIPTION

The VDU-K fits into an Interak 1 computer and provides the means for the user to view output data from the computer. However the VDU-K is also described as an "Applications" VDU, in that it can provide the visual output for numerous applications to which a computer may be put. For example a dedicated chess-playing computer could use the VDU-K with a pre-programmed set of chess pieces, or other applications may be a set of named pictures to help children in their reading, or a set of electronic components for electronic circuit design, or graphic displays of animals for computer controlled feeding etc. in animal husbandry. Many of the applications to which the VDU-K can be put have been known for many years but it has been too expensive to devote a whole computer to a fairly simple application. Extremely low-cost displays are possible because the VDU-K is designed to give excellent results on a standard T.V. receiver.

For some applications more than one display screen is required and the VDU-K can satisfy these by a simple adjustment to the address selection links or switches to allow more than one card to be plugged into the same system.

Although the VDU-K is designed to fit into the Interak 1 computer it is a standard size (4.5 x 8 inch) card which can be incorporated into other computer systems. To these computers the VDU-K card simply looks like 1K of RAM (read/write) memory, the first 768 locations of which are displayable on the T.V. screen. In a manner of speaking the T.V. screen is like a "window" through which the contents of a portion of the computer memory can be examined. If the computer program wants to display a message or picture for the user to see it simply writes the codes for the appropriate data into this area of RAM, and they are displayed on the screen by the VDU-K.

For alphanumeric data such as the letters of the alphabet, numbers, and punctuation, a suitable well known code exists, the American Standard Code for Information Interchange, or "ASCII" for short. In this code the capital letters of the alphabet, A, B, C, etc. (for example) are represented by the computer codes 41H, 42H, 43H, etc. (the suffix "H" means that these numbers are the hexadecimal numbers often used in computer work, rather than conventional decimal numbers).

The computer reads or writes the data stored on the VDU-K card in the form of an eight-bit byte, at one of 64K different locations or addresses (64K = 64 x 1024 since 1K = 1024; do not confuse this with 1k which = 1000). The total memory on the VDU-K card comprises 1K such locations, although only the first three quarters of them are visible on the screen. The 1K memory on the VDU-K card can be sited at any one of 64 different locations (known as 1K boundaries) within a 64K system, and can be selected by altering the position of six wire links or DIL switches (there are 64 different arrangements of these six selection links or switches since they each can have two positions and $2^6 = 64$).

As the data are in the form of eight bit bytes there are a total of $2^8 = 256$ possible different characters. These are held in two 2K EPROMs, U24 which holds the first 128 characters, and U23 which holds the next

128. As EPROMs get cheaper and cheaper it may happen that the 4K type 2532 or 2732 may be more economic than a pair of 2K types. The card is laid out so that a single 4K EPROM can be used in place of the pair of 2K ones. As the 2532 and 2732 are not pin compatible a jumper area (P5) has been provided so that either may be fitted.

In normal circumstances only one 2K EPROM is fitted at first. The ASCII code is a seven bit code and so there are only $2^7 = 128$ possible different characters in that set, in fact there are less because many of the ASCII codes are "non printable" e.g. carriage return, delete, back-space etc. The standard 2K character generator EPROM for this board contains mostly the printable ASCII codes, but some special characters have been included as well, especially for the "non printable" codes. When only this single character generator is installed the remaining 128 codes are not wasted. Instead a switch option is selected so that the second 128 set of characters are the same as the first but presented in reverse video, i.e. white appears as black and vice versa. The use of reverse video is useful for dramatic warnings and headings on a displayed screen, and is also often used to indicate the position of a screen cursor which would otherwise obliterate any character in whose position it was resting.

If the standard character generator is installed then the second character generator which may be fitted to give 128 totally different characters (rather than simply the reverse video version of the first 128), is described as the "Applications Characters" EPROM. It is called this since the contents of this generator will depend on the precise application to which the VDU-K is being put. Of course "Applications" charactors could be put in the first EPROM as well, but this is thought of as being unusual on the grounds that there are many applications which require the use of alphanumeric characters for messages, labels, etc. and it suits everybody's convenience if these standard characters are to be found in a standard position.

A design for a "Programmable Character Generator" is now available, and the production of a suitable printed circuit board is under consideration. In the design a RAM-based character generator is connected via ribbon cable to the "Applications Characters" EPROM socket. This provides 128 characters which can be defined and redefined as a program runs, and can often give the illusion of high resolution graphics.

A further application for the VDU-K is to act as a test-bed for other screen formats, for example usable results with a 64 character line have been reported. This is not supported by the designers of the card however because of the reappearance of the "snow" effect.

Although the card has been designed with a television receiver in mind for economy, components have been included so that a T.V. Video Monitor (composite video) can be used as well if desired. An on-board modulator is used for the standard T.V. receiver output. The modulator used gives first-class results, but suffers from the disadvantage that it requires a non standard video signal, so this is produced on the card in addition to the "normal" video signal.

A unique microprocessor controlled T.V. sync. generator circuit has been adopted, and as a result it has been possible to provide a switch option to choose between an interlaced and a non-interlaced display.

Full buffering has been included so that no more than one input connection is made to any of the edge connector lines. Operation with a Z80A at a full 4 MHz without "wait" states is possible (and recommended for no "snow"), but the card can be used with certain other microprocessors. It is very simple to use in that it requires only an address bus (with memory request if appropriate), a data bus, and the read and write control strobes. The Z80A refresh signal has been included however to ensure that the VDU-K does not respond to a dynamic RAM refresh address. Power requirements are all met by a single +5V supply.

The mechanism whereby the data are converted to a form where they can be displayed on a T.V. screen is discussed in detail later in this Manual, but a general description is as follows: The eight bit bytes representing the characters which are to be displayed are stored in the RAM on this card. This RAM is known as the "video" RAM. A set of multiplexers connect the RAM addresses to the microprocessor bus should the microprocessor require to read from or write to the video RAM, but most of the time the multiplexers connect a counter chain (derived from a crystal oscillator) which is cycling round continuously during the time a picture is being displayed. As the counters cycle they present first one address, then the next, and the next, and so on, in turn to the video RAM. As a result the data contained in each of the displayable RAM locations are output byte at a time in sequence by the video RAM. If for example the letters A, B, C, were to be displayed the codes would be (for the standard ASCII charactor generator), 41H, 42H, 43H, one after another. These output data codes are presented as addresses to the character generator EPROM which is programmed with the pattern of 0's and 1's which are to be transmitted to the T.V. screen. Since a T.V. picture is made up of individual dots the eight bits of character information data from the EPROM are loaded into a shift register and clocked out by the "dot clock" a dot at a time while the EPROM is producing the pattern for the next character.

Each character such as the letter A, for example, is made up from a number of horizontal rows of dots arranged vertically above one another. In this case there are ten such rows or "picture lines" for each character. This means that the EPROM character generator must be accessed as described above ten times for each character displayed. This is done by having a picture line counter which provides an additional address to the EPROM. Only after ten picture lines are dispayed does the count proceed to get the next set of characters from the video RAM.

The output of the shift register is added to, and synchronised with, the timing information from the T.V. sync generator to provide two composite video signals, one of which can drive a T.V Monitor, the other of which can drive an ordinary T.V/ receiver, via an on board modulator.

This concludes the general description of the VDU-K circuit.

2.3 SWITCH SETTINGS, EPROMs, OPTIONS, etc.

DIL Switches

There are two positions on the card where DIL switches may be fitted, S1 and S2. DIL switches are not supplied in the standard kit of parts as they are fairly expensive and many users will prefer to make other arrangements. However DIL sockets for both S1 and S2 are supplied. It will be assumed for convenience of writing that switches have been fitted, but there is no reason why the connections could not be made some other way, for example DIL pin headers, or wire links, perhaps on the track side of the board.

S1

It is in fact recommended that no switch or links be fitted on the board in position S1, but the type of DIL switch which could be used here is DPDT (double-pole, double throw); great care should be excercised if the more common type of DIL switch is used instead (i.e. 2 x SPDT) as it is quite easy to short one of the signals to ground, possibly with damaging consequences. The recommended method is to use instead the two sets of 3-pole connection pins P1 and P2, to connect a front panel mounted DPDT switch. Sheet 6 of the circuit diagram in section 5 of this Manual shows S1 and the alternative connections.

The purpose of the switch is to permit the user to have control over the function of the eighth bit of the VDU data. If a single character generator is in use, giving a standard set of 128 characters, then the eighth bit can be used to provide a duplicate set, but in reverse video. The setting of the switch is marked on the diagram as "REV". So for example if this setting was chosen and the data 2A (hex.) and AA (hex.) were written to the VDU RAM then 2A would normally result in a white asterisk (*) being displayed on a black background, whereas AA would result in the same character being displayed as black on white. This is because AA has the same seven low bits as 2A, but has the eighth bit set to "1".

If a second character generator (the "applications" character generator) is in use then the switch should be set to the "ALT" position if it is wished that the eighth bit select one of the alternative 128 characters. Taking the same example as before, 2A would be the same asterisk in normal non-reversed video, but this time AA would be whatever character had been programmed into the second EPROM, e.g. a chess-piece, or some other graphics symbol.

It might be thought that if a second character generator is in use then the front panel switch described is redundant. This is not the case, because many programs rely on the eighth bit being simply a reverse-video control bit. One notable program which needs this is ZYMON for its cursor, and it is also often used in Text Editing programs say to highlight a block of text before it is moved or deleted. It is suggested that the switch be left normally in the "REV" position, and only moved to "ALT" when it is desired to use the characters in the Applications EPROM (if fitted).

S2

A 16-pin socket is provided for S2, which should be an 8 x SPST type if a DIL switch is used. We can therefore refer to eight switches S2a to S2h; S2a connecting pins 1 and 16 of the socket, if the pins are counted in the same way as for a 16-pin I.C.

The first six switches S2a-S2f choose on which of the 64 possible 1K boundaries the VDU-K memory is to be located. S2a is the MSD (most significant digit) and corresponds to the chosen state of address bus line AB15; the other switches continue in sequence until S2f is reached, which corresponds to AB10. Note that due to the fact EX-OR gates are used to select the chosen address (see circuit diagram Sheet 3), the complement of the address should be set on the switches, i.e. for an address with a "1" on a given line, the corresponding switch should be set to "0", by turning that switch ON. For example for use in an Interak 1 system with a ZYMON 2 monitor, the VDU RAM has to begin at address F000 hex. The most significant bits of this number in binary notation are 1-1-1-1-0-0, and so the required settings for S2a to S2f are ON-ON-ON-ON-OFF-OFF respectively.

The next switch, S2g, is used to alter the VDU-K circuit to suit some types of microprocessor other than the Z80A-CPU, notably those types which do not provide an NMREQ signal like that of the Z80A-CPU. By closing this switch for this type of microprocessor, e.g. INS-8060, SC/MP, it is sometimes possible to reduce the time of the CPU access so that the "no snow" feature of the VDU-K is retained. For Z80A use in the Interak 1 system S2g should be left OFF.

The final switch is S2h. This is to be found on circuit diagram Sheet 2. It alters address line A9 on the timing generator EPROM U2, and so selects an alternative timing program, if one is provided in the EPROM. In the case of the first standard EPROM supplied for U2, S2h in the OFF position selects a timing program for a non-interlaced display, and S2h in the ON position selects a timing program for an interlaced display. Most people seem to prefer the non-interlaced display once they have seen both, and so they will leave S2h OFF.

Summary of S2 Switch Positions for Interak 1 Use:

Set S2a-h ON-ON-ON-ON-OFF-OFF-OFF-OFF respectively.

S3

S3 is a further optional switch or link. If a switch is used it should be a SPST type, mounted preferably on the front panel. The switch is connected between pins 1 and 2 of pin assembly P4. It is shown on Sheet 7 of the circuit diagram in Section 5. Normally the switch is closed, and the normal characters appear as white on a black background, reverse video characters being black on white. At all times with S3 closed the top bottom and side margins on the screen are black. The function of S3 open is to "Reverse All", i.e. the top bottom and side margins and the normal screen are all white, and normal characters now appear as black on a white background, with

reverse video characters now being white on black. It is suggested that consideration be given most seriously to choosing this latter option. In many applications, particularly those where the screen is viewed by people who do not usually use computers, the "Reverse All" option will often meet with wider acceptance. One reason is that people are accustomed to reading the printed word as black on white, and another is that the dots which make up the characters are not dots at all when they are black; they therefore appear to make more attractive "joined up" characters.

It is worth-while having a front panel switch because the white background can become a bit overpowering when viewed for long periods, and the hardened computer user will usually find the black background more restful on the eye.

UHF/Video

There is space on the card for the fitting of a UHF modulator type UM1233 E36, to provide an output suitable for connecting to the aerial socket of an unmodified television receiver. Even though many users may have access to a video monitor, it is suggested that unless funds are really short the UHF modulator always be fitted. This is because in the event of a breakdown to the UHF monitor, work with the computer can still proceed if a T.V. set can be found. This is a similar recommendation to that in the motoring world where motorists are advised to carry and maintain a spare tyre, and of course this advice may be disregarded. The connection to the modulator can be taken directly from the phono socket output of the modulator (use a phono plug with the centre pin cut short), or more elegantly from a Belling-Lee (T.V. Aerial) connector on the front panel. Special screening arrangements are desirable in the latter case, which are discussed in the Constructional Notes section of this Manual (Section 3).

The VDU-K card also provides a composite video output of a couple of volts peak to peak, for direct connection to a video monitor. This output is independent of the signal used on the card for the UHF monitor and it is therefore very easy to change over from T.V. to Monitor and back again, indeed to run both if required. The connection point is P3 on the card, the signal being taken from pin 1 of P3. Screened cable should be used, the screening being taken to pin 2 of P3. It is suggested that a front-panel BNC Connector be used for the Video output.

EPROMs

These have already been mentioned at intervals throughout the Manual so far. They are two or three in number, identified as U2, U23, and U24.

U2 is a 2516 or 5-volt 2716 type, preprogrammed with one or more programs which are used to form a timing generator. A standard preprogrammed EPROM can be obtained from the supplier of the VDU-K card, included in the kit of parts, or separately, ordered as "Timing

Generator EPROM". U2 is shown on Sheet 2 of the circuit diagram, and it will be seen that its address line A9 (pin 22) is connected to S2h. As already mentioned, the usual purpose of this switch is to select an interlaced or non-interlace display format. Address line A10 (pin 19) is hard-wired to 0V, but the circuit board track can be cut so that A10 can be wired to +5V instead, and so release a second pair of timing programs, for example for a 64-character by 16-line format. 3 holes have been provided in the circuit board close to pin 19, so that a 3-pin assembly can be fitted to connect pin 19 of U2 to either 0V or +5V (never both!).

Some brief information on the way the Timing Generator Program is written is given in Section 4 of this Manual, and it likely that a listing of the program will be made available at extra cost.

U24 is a 2516 or 5-volt 2716 EPROM which contains the 128-character "Standard Character Set". This is supplied in the kit of parts or may be purchased separately as "Character Generator EPROM". In normal circumstances an EPROM is always fitted as U24.

A second group of 128 characters can be contained in a second 2516 or 5-volt 2716 EPROM. This is known as the "Applications Character Set", contained in the "Applications EPROM". These characters can be defined by the user (see Section 4 of this Manual for details), or some sets will be made available for sale for certain applications, e.g. "Chess Pieces". If used the Applications EPROM should be fitted as U23.

The types of EPROMs described so far have all been 2K in length. At the time of writing (Summer 1982) 2K EPROMs have, perhaps surprisingly, become less expensive than 1K types. It is conceivable that some time in the future a 4K EPROM may similarly become less expensive than the 2K types. To provide for that contingency, the VDU-K card has been arranged so that instead of two 2K EPROMs for U23 and U24, a single 4K EPROM can be fitted instead. This would contain 256 characters, i.e. both the Standard Character Set and the Applications Characters. If a 4K EPROM is used it should be fitted as U24, and the socket for U23 left empty.

There are two common types of 4K EPROM: the 2532, and the 2732. Unfortunately they have slightly different pin arrangements. The 2532 is close enough to the 2K types to fit in directly without any circuit changes (the VDU-K card has been carefully designed to permit this - it is by no means generally the case), but the 2732 needs some circuit changes. The alterations are all carried out on the 5-pin 0.1" pitch pin assembly P5. For all EPROMs discussed except the 2732, link pins 1 and 2, also (and separately) pins 3 and 4, on P5. For the 2732 link pins 2 and 3, and also (and separately) pins 4 and 5. Note that if some sort of plug-in arrangement is made it is a simple matter of turning this arrangement through 180° to accommodate the different EPROM, i.e. it is either the upper two pairs of pins which are linked or the lower two pairs.

10/16 Line Counter

Each of the displayed characters is normally an arrangement of the 80 dots which make up the 8 x 10 matrix (Further details are included in Section 4 of this Manual). The vertical parameter of this matrix, the 10 picture lines, is set by the decade counter U10, which is a 74LS290 device. This has been deliberately chosen in place of the older 74LS90 for two reasons: Firstly because it is the type now recommended for new designs, having the supply pins in the conventional positions, at the corner pins, and secondly because fortuitously it is pin-compatible with the binary counter type 74LS293.

If the 74LS293 is substituted for the 74LS290 as U10, the character matrix is extended vertically, and becomes 8 x 16. This is not normally usable, because with the normal 24 rows of characters the number of picture lines used (24 x 16 = 384, or 768 on an interlaced display) exceeds the number available on a standard T.V. (312 lines non-interlaced, or 625 lines interlaced).

However, for special applications, for example if the number of rows of characters (normally 24) is reduced to 16, e.g. for a 64 x 16 display, or perhaps for some graphics experiments, then an 8 x 16 character cell matrix has some attractions, since 16 rows of characters each of 16 picture lines occupies 256 lines in total (512 interlaced), which conveniently fills the screen almost from to bottom.

Some people certainly favour a tall thin matrix for alphanumeric characters, considering that they look less like those used in childrens' books (i.e. short fat characters).

If experiments along these lines are to be conducted, then some attention will be necessary to the Timing Generator EPROM to reduce the top and bottom margins, and increase the picture area.

This concludes the discussion on the various options open to the user of the VDU-K card.

2.4 DETAILED DESCRIPTION

The circuit diagrams in Section 5 of this Manual will be taken as the basis for the detailed circuit description. The Manual is already in danger of becoming inconveniently long, and so it will have to be assumed that a certain amount of background knowledge is possessed by the user.

Mostly, the components on the diagrams and in the parts list use the designation letters specified in ANSI standard Y32.2-1970. In a way these letters are fairly irrational (e.g. "J" is a connector, "Q" is a transistor, "U" an integrated circuit, and so on), however as it is a standard it has been adopted here. The component overlay diagram uses the same designations as for the circuit diagrams.

A block diagram is provided, which also serves as a "map" showing the user where he may find the particular section of the circuit in which he has an interest. Each of the sections represent a logical unit of the whole circuit. Particular care has been taken when preparing the diagrams to ensure, as far as is reasonably possible, that the diagrams begin at the top-left hand corner of the drawing, and continue downwards from left to right. Another convention which has been followed as rigorously as possible is to have the inputs to the left of each circuit block and the outputs to the right. Although this is a very logical and sensible approach to drawing circuit diagrams, it is surprising how often these ideas are disregarded.

In order to include the information which it is desired to present on the circuit diagrams (pin numbers, function names, power supply pins etc.), it has been necessary to use several sheets of paper. However great care has been taken in partitioning the diagram to turn this apparent disadvantage into a positive advantage, by breaking the circuit up into individual sub-functions which are more easy to understand a step at a time. Even the order of the various sheets has been given close attention, so that as far as possible the source of a signal is shown on an earlier diagram before it used on a later one. All signals which connect to a part of the circuit on a different page are given names, and their source or destination is shown in the form (e.g.) SIG1 3/10,12(4);6/9(5). This example means the signal called SIG1 is connected to U3 pins 10,12 on the circuit diagram sheet (4), and also U6 pin 9 on sheet 5 of the diagram.

So as not to interfere with the logic flow, not all power supplies are shown on the integrated circuits drawn. Instead, each sheet of the diagram contains a table of the integrated circuits on that sheet, their type number, and their power supply connection pins. This does not apply to power supply connections which represent a logic level input, for example 0V for a logic "0", or +5V for a logic "1"; these are shown connected to the integrated circuit pins. An effort has been made to show all pins of each integrated circuit, even the ones which are not connected to anything else. Such pins are marked "N.C.", which means "not connected".

The Parts List is to be found at the very back of the Manual, for easy

reference. It is organised in two ways; firstly by component reference number, which gives the component value if the reference number is known, and secondly by component value, which gives the reference numbers of all the components which have that value. The latter method is more convenient when checking a kit of parts and assembling the card, for example it is often useful to know where all of the components of a given value should be located if you finish construction and find one or two items left over. Later, you will want to know the value of a component of a given reference number, and the first method of forming the parts list will be more appropriate. To minimise the well known chore of searching all over a circuit board seeing if you can find say C11, or R17, which have become temporarily invisible, the components on the component overlay have been numbered in ascending numerical order starting at the top left-hand corner and working across and down to the bottom right. (So if you are looking for an elusive R17, you will know you are getting warm if you see R16 or R18 - R17 won't be far away.)

To help users carrying out tests on the card, or wishing to modify it, both ends of such components as resistors and non-polarised capacitors are identified on the circuit diagram, for example if it is wished to check the reset pin of U1 (on sheet 2 of the circuit diagram) it can be seen that it is connected to end 2 of R9, end 1 of R9 being connected to +5V. On the component overlay diagram horizontally positioned components should be taken as having end 1 to the left and end 2 to the right, whereas vertically positioned components should be taken as having end one to the top of the diagram, and end 2 to the bottom. In an effort to help users all components have been placed on the card in a similar direction, so that for example all the I.C.s are the same way round, similarly the electrolytic capacitors and diodes.

Section 5 also includes various timing diagrams, which may be an aid to understanding certain parts of the circuit.

As the circuit diagram has been drawn split up into logical blocks, these represent convenient sections into which the circuit description may be divided.

Sheet 1. The Block Diagram.

This shows the complete circuit in block form. In Sections 2.1 and 2.2 of this Manual general descriptions of the way the card works have been given and it is now time be more specific. The Block diagram is a little like having the whole circuit diagram on one page, and is of course fairly comprehensive as a result. Once it has been studied it should be thought of as a "map" showing where to find the detailed diagram corresponding to each block, and to this end the appropriate sheet number of the circuit diagram is given beneath each block.

The essential function of the VDU-K card is to provide what can be termed a "window" into the memory of the computer system. It has a "1K Video RAM" (shown on the block diagram slightly below right of centre) which can be written to and read from, similarly to any of the other RAM in the system. The significant difference is that the data in this RAM are also being continually processed on the VDU-K board in

such a way as to render them visible when viewed on a T.V. or video monitor screen. A fair amount of circuitry is necessary because of the demands of the T.V. system, which requires 50 complete screenfuls of information per second, correctly organised into a composite video waveform having the appropriate pattern of dots correctly synchronised with the required frame and line synchronising pulses. In very cheap systems some of the burden of this activity is borne by the system microprocessor, with an inevitable reduction in performance of one kind or another, but on the VDU-K it is all carried out on the card, and the main system microprocessor is not slowed down or restricted in performance in any way.

The block immediately preceding the 1K Video RAM is entitled "Multiplexer". This is the technical term for the circuit which switches the address lines over to the System "Address Bus" when the microprocessor is programmed to read from or write to the Video RAM. The appropriate signal is given to the multiplexer by the output of the "Address Comparator and Control Logic" block, which is set up (by selection links or switches, and various gates) to give the signal when a read or write of the Video RAM is required. At the same instant the "Monostable" is fired, which immediately freezes the "Octal Transparent Latch" to ensure that the data which were previously coming from the Video RAM, and which are destined to be viewed on the screen, are held safe while the microprocessor read or write is carried out. It is is this latch which is central to the method used on the VDU-K card to produce "no snow".

The "Octal Data Bus Transceiver" is "enabled" at this time and connects the data bus to the data lines of the Video RAM and the read or write is carried out. (The tranceiver has a direction control, not shown on the block diagram, which sets its read/write direction appropriately). Although these data are also presented to the inputs of the "Octal Transparent Latch" its outputs are unaffected as they are held latched by the signal from the monostable.

After the microprocessor read or write is over, the multiplexer reconnects the Video RAM to the on-board addresses which are looking after the supply of correct information to the screen. Fast RAMs are used and soon the data outputs from the RAM are correct for feeding on to the screen. The monostable is arranged to "time out" just after the data are correct, and so render the octal transparent latch transparent again. The timing of the circuit has been worked out most carefully to ensure that with a Z80A-CPU microprocessor operating at 4.0 MHz, there is never any disturbance of the displayed picture even if the microprocessor is continually accessing the Video RAM. The various timing diagrams in Section 5 includes one which shows how the method works, and one which illustrates the timing for the "block move" instruction of the Z80A-CPU. This is the most stringent of all for the VDU-K, since it involves the Z80A-CPU issuing a consecutive read and write without the normal breathing space when the op-code is fetched or re-fetched.

The above part of the Block Diagram has been covered first, perhaps out of its logical order, so that all of the above points can be assumed known in what follows.

The top left-hand corner of the Block Diagram will be taken as the starting point for the remainder of the Block Diagram description.

This shows the "12 MHz Oscillator", which is crystal controlled by a 12 MHz quartz crystal. In fact 6.0 MHz is the maximum frequency required on the VDU-K card, but twice this frequency has been chosen to make life easier for any users who are carrying out experiments to double the clock rate, for example to obtain a 64-character format.

The 12 MHz is divided by 2 to give a 6 MHz signal which is used as a "Dot Clock", and further divided to provide various other signals, and a 3 MHz signal is obtained to be the input to the "Active Pull Up". The active pull up transforms the logic "1" level from the normal TTL value of 2.5-3.5 volts to near enough a full 5 volts (it also inverts the signal in the process but this is immaterial). It is a great shame that the miracle of integration which puts 40,000 transistors on a chip in the Z80A-CPU does not extend to providing as well the extra transistor Q1 which is used for the active pull up.

The output of the active pull up is used as the clock input to the "Z80A-based T.V. Sync. Generator". This is, as far as is known, a unique design which is an excellent example of how a two-chip microprocessor system (the Z80A-CPU and the 2716 EPROM) can give cost and space savings and yet provide performance advantages over more conventional designs. There is no need for any RAM here as there is sufficient contained within the registers of the Z80A-CPU itself. If anyone is sufficiently impressed to copy the idea themselves, they are welcome to do so; we will be less likely to get cross however if they make it clear where they first saw it!

The choice of 3 MHz is no casual choice; one of the time intervals in the C.C.I.R. television standards, which is the basis of those we use in this country, is 2.33 microseconds. This is 7 Z80A "T" states at a clock frequency of 3 MHz, which is very convenient because 7 "T" states is the time it takes to execute many of the instructions in the Z80A set. At this clock frequency one picture line (64 microseconds) is exactly 192 "T" states. There is a little more on this subject in Section 4.3 of this Manual.

Referring again to the "Dot Clock", it should be noted that although this is 6 MHz, it does not mean that the dots on the screen are issued at this frequency. The maximum equivalent frequency of the dots is when they are alternately black, white, black, white, and so on. Since they come from a shift register which is being "clocked" at a 6 MHz rate, i.e. six times per microsecond, they will be dots of one sixth-microsecond duration. The frequency of a signal which is say black for one sixth of a microsecond then white for one sixth of a microsecond before it goes back to black again, is in fact only 3.0 MHz, since the period of the waveform is one sixth plus one sixth, making one third of a microsecond, i.e. frequency 3 MHz. As the waveform to produce the dots is a squarewave it requires a much greater bandwidth than 3.0 MHz for accurate reproduction. The T.V. set video bandwidth is about 6.0 MHz, which proves sufficiently wide to give a first-class picture, and so avoid the expense of a video monitor unless one is already available.

The next block to be mentioned is the "32-Character Counter". This counts a signal which has a duration equal to each one of the displayed character cells, and the outputs are presented via the multiplexer to the address lines of the Video RAM. In this way 32 sequential locations in the RAM are selected in turn, and provide data which are ultimately directed to the display.

The next block is the "10-Picture Line Counter" which advances by one each time a count of 32-Characters is completed. This continues until all 10 picture lines have been counted. As each picture line is counted the same set of data is provided by the Video RAM. The same data are used because the characters are 10 picture lines tall, and 10 identical passes through the video RAM are necessary to build up each complete row of 32 characters. Although the characters remain the same for each 10 picture lines the dots making up those characters do not, and so the 4-bit outputs from the 10-Picture Line Counter are connected to the Character Generators. More will be said on this subject when the character generators are discussed.

After 10 picture lines have been counted it is time to proceed on to another row of characters on the screen, so after 10 counts of the picture line counter the "24-Row Counter" is advanced by one. The outputs of the row counter are used as further addresses in the video RAM, and a whole new set of data is issued for each count of the 32-Character counter. As before, this new set of data is repeated for 10 consecutive picture lines, at which point the row counter is advanced by yet another count and another new row of data is addressed in the video RAM.

After the final picture line of the 24th Row is complete, all of the counters are reset by signals from the Z80A-based T.V. Sync. Generator, ready to begin again for the next T.V. picture "frame". It is implicit in the method that the whole sequence repeats regularly fifty times a second, to provide the illusion of a permanent display on the T.V. or monitor screen. The display is of course made up in the same way as any T.V. picture, i.e. by controlling the output from an electron beam as it is rapidly scanned down the screen, line by line. It is essential that the motion of the beam is precisely synchronised with the output from the VDU-K so that each time the picture is retraced it is in exactly the correct position. For a non-interlaced display successive "frames" should be in precisely the same position, and for an interlaced display successive frames are moved alternately up or down by half the distance between lines to give the illusion that there are twice as many lines on the display.

The standard T.V. Sync Generator produces all the necessary sync. pulses for interlaced and non-interlaced displays, to force the television or monitor to begin its electron beam scan at just the right moment.

The final few blocks on the Block Diagram are at the foot of the page. The first is the "EPROM Character Generator(s)". The "Select Switch" chooses whether a single 128-characters plus their reversed set are used or a full 2 x 128-characters are to be used, by adding tha "Applications EPROM". The EPROM used has inputs to its address lines

and is programmed with carefully chosen corresponding data at its output lines. The higher order address lines come from the data outputs of the video RAM, and the lower order address lines come from the 10-Picture line counter.

As the 32-Character counter cycles rapidly through the addresses of a row of characters, the corresponding data in the video RAM are presented to the character generator EPROM as addresses. The characters can be the same or different, but whatever they are they each provide access to a unique block of addresses within the EPROM. The individual addresses within the block are provided by the picture line counter, so that as it counts it can access the data needed for successive lines.

The pattern of dots which has been programmed in the EPROM to correspond to the particular character code, and just as importantly to correspond to the precise line of dots within the character cell, is output on the eight data lines of the EPROM, and loaded in parallel into an eight-bit shift register just before the character counter proceeds to the next character address. The shift register is "clocked" continuously at a 6 MHz rate and while it is providing the eight dots for the current character there is time for the next group of eight dots to be obtained from the EPROM.

The block marked "Synchronisation" includes the circuit which brings together the video signal (the pattern of dots) and the T.V. sync. pulses, converting them to two "composite video" signals. One of these is suitable for driving the final block the "UHF T.V. Modulator" which provides a signal suitable for direct connection to a T.V. aerial socket, and the other is slightly different in level and is suitable to connect to a T.V. monitor which accepts a composite video signal of a couple of volts peak to peak.

Another function performed by the earlier block "Synchronisation" is to ensure that the signals which gate the dots are exactly timed, so that for example the reverse video signal and the signal which defines the left and right hand margins coincide exactly with the start and finish of the individual dots. If this is not done the display can show unwanted "ghost" dots in certain positions, and exhibit annoying discontinuities where characters adjoin.

This concludes the Block Diagram Description. We are now in a position to proceed to the detailed description of the individual sheets of the circuit diagram.

Sheet 2: Oscillator, Dividers, and Sync. Generator.

Starting at the top left hand corner of this diagram two inverters type 74S04 form a cross-coupled multivibrator having a crystal in place of one of the capacitors. This constrains the circuit to oscillate at the crystal frequency. A 74S04 is used rather than the more common 74LS04 because experience with this particular oscillator circuit has from time to time in the past not been entirely satisfactory when certain combinations of crystal and 74LS04 have been

used. A further 74S04 inverter acts as a buffer for the 12 MHz signal, so that an oscilloscope probe can be used during test without disturbing the operating conditions of the oscillator. U14 is a 74LS393, a dual binary ripple counter which divides the 12 MHz by successive powers of two. Note that the first section has its reset line permanently earthed so it is simply a divider, whereas the second stage has its reset pin 12 connected to the reset signal R, and so it is acting more like a counter, starting from a fixed point, all zeros. Some of the signals so far discussed are included on one of the timing diagrams, but they will be mentioned again in the description of the diagram on sheet 6.

A 74S04 drives the Z80A-CPU clock input from a signal called "3 MHz", and Q1 is a general purpose PNP transistor which is used as an active pull-up to ensure that the clock signal rises sharply to nearly +5V when required (this being a special requirement of the Z80A-CPU clock circuit which unfortunately is not guaranteed to accept a normal TTL level clock). R8 limits the base current to Q1, C8 provides increased transient drive to turn Q1 on more quickly, and also removes excess charge from the base to turn Q1 off quickly a short while later. R7 assists in this latter endeavour. C8 is sometimes called a "speed up capacitor" because of its purpose. R3 limits the current which passes through Q1 on those inevitable occasions when for a brief instant U8 pin 8 is conducting to ground and Q1 is conducting to +5V. Rumour has it that R3 also plays a small part in tailoring the rise and fall time of the waveform to suit the Z80A-CPU specifications.

U1 and U2 represent a small microprocessor system dedicated to the task of producing all of the specialised timing pulses, most notably the complicated T.V. Sync waveforms for interlaced and non-interlaced displays. A timing diagram for the various pulses produced is included in Section 5.2 of this Manual. Some of the inputs to the Z80A-CPU (pins 16, 17, 24, 25) are strapped high via resistor R6. These are inputs which are not used in this simple sub system. The reset line U1 pin 26 is held high by R9. At power on C11, which is also connected to pin 26, is discharged and holds the Z80A-CPU reset so that it starts executing its control program, held in U2, from a known point, once correct operating conditions (power supply, clock, etc.) are established. Once C11 has charged sufficiently (via R9) the reset condition is released, and U1 begins its normal operation. The purpose of CR1 is to discharge C11 quickly when power is removed, so that it will be ready to provide a power on reset again if power is restored quickly, also CR1 provides a direct discharge path for C11 when power is removed to prevent C11 discharging into pin 26 of U1. In the interests of economy no limiting resistor has been provided in series with C11, so a diode with a good surge rating has been specified for CR1.

Only two control strobes from the Z80A-CPU are used, Read (pin 21), and Write (pin 22). Such signals as $\overline{\text{MREQ}}$, $\overline{\text{IOREQ}}$, $\overline{\text{BUSAK}}$, $\overline{\text{M1}}$, $\overline{\text{RFSH}}$, are entirely superfluous in this application and no connection is made to these outputs. There may be more than one control program held in U2 (selected by altering the levels on U2 pin 22, and U2 pin 19, one via S2 pins 8,9 and the other via a cuttable circuit board track), but none of them exceeds 0.5K in length, therefore the nine Timer Address

Lines TA0 to TA8 are sufficient, indeed in this case the partial addressing is beneficial because the program is always constrained to run in the single 0.5K space, and is less likely to get "lost" (through e.g. supply line transients, inadvertant short circuits with test probes and the like). Whenever a read is carried out, i.e. an op-code fetch, the Read line goes low and enables U2, the only memory device in this small system. The data flow along the Timer Data bus TD0 to TD7.

At the appropriate instant, accurate to the exact "T" state, suitable data will be written to the hex D-type flip-flop U13, type 74LS174. As only four signals are required, there are two lines spare for some alternative needs which may arise. According to the precise data written to U13, and their precise timing, all of the signals needed on this card can be synthesised, saving a money and board space, and as a bonus permitting much improved flexibility. The four signals are called V, H, R, and S. They are drawn on the timing diagram in Section 5 of the Manual, but it is appropriate to mention their purpose now.

"V" is a signal which resets the vertical counters (picture line, and character row). The signal is high during the top and bottom blank margins on the screen, resetting the counters (see Sheet 4), and goes low in the active picture area letting the counters count out the number of lines, and character rows.

"H" is the horizontal picture enable signal. It is low during the top and bottom blank margins, blanking the picture throughout these lines, and during the active picture area it goes high for a 42.66 microsecond interval during each line, 42.66 microseconds being the exact time necessary to display 32 whole characters at the chosen dot clock frequency, the space on each side defines the left and right hand picture margins.

"R" is the reset signal. It is immaterial what level it is during the top and bottom margins, since nothing is being displayed at this time (but the present version of the Timing EPROM sets it high in the top and bottom margins). Its main purpose is to reset the 32-character counter immediately before the active part of the H signal on each displayed picture line. These counters are not left running as they have to begin at zero at the start of each displayed line in order to count out the 32 characters in the same order for each and every displayed line. The size of the reset pulse is not critical, and it happens to be convenient to make it 8.66 microseconds, in at least one version of the Timing Generator EPROM.

"S" is the much discussed T.V. sync. signal. A glance at the waveform diagram will show it is particularly complex at the start and finish of each frame, but during the top and bottom margins and the central picture display area it is a simple regular pulse. The C.C.I.R. standards require it to be a 4.66 microsecond pulse repeated every 64 microseconds, i.e. at the start of each and every picture line.

Two of the inverters in U8 are uncommitted, and they are shown at the foot of Sheet 2 of the Circuit Diagram.

Sheet 3. Address Comparator and Control Logic.

The upper six bus address lines, AB10 to AB15, are compared with the six address selection switches (or links). The switches must be set to the complement of the desired address. This is fairly easy to remember since this result in the switch to be ON for a ONE in the chosen address, and OFF for a ZERO. The detailed switch settings have been discussed in Section 2.3 of this Manual. When the address on the bus matches that set on the switches as described, the outputs of all the open collector EX-OR gates (U7 and U12, type 74LS136) which are wired together go high. It is a unique selection since a mismatch on any of the lines would cause the output of that EX-OR gate to go low, so pulling down all the others. It should be noted that the action described so far is all conditional on U12 pin 4 being low at this time. It will be low provided both inputs to U5 (pins 9 and 10) the OR gate which precedes it, are also low. In turn this means that the refresh line has to be high, and memory request has to be low. These latter conditions prevent the VDU-K card responding if it happens to be set to an address which is present on AB10-15 during either Refresh or an I/O transaction. (For Z80A-CPU use S2 pins 7 and 10 will be open, enabling U6 pin 9.)

For other processors, which do not provide or simulate the Z80A-CPU NRFSH line, a position is provided for a resistor R21 which will hold this line high if required. Also some other processors may issue their address so early in their read or write cycle that the microprocessor access to the VDU memory may be prolonged unduly, so causing "snow" on the screen. An example of such a processor is the INS-8060, or SC/MP. If this is in use S2 pins 7 and 10 should be closed. This will prevent the address match being found until either a read or write strobe is actually present, much later in the cycle. (This is achieved via the action of the output of U5 pin 3, which only goes high when a NWDS or NRDS strobe is present. Before this its output is low, which forces U6 pin 8 high, hence U5 pins 9 and 8 and thus makes U12 pin 6 low, preventing a match of any addresses.)

Once a match is found the signal SELMPU goes high, $\overline{\text{LATCH}}$ goes low and the monostable U3 is fired which will prolong the $\overline{\text{LATCH}}$ signal even when SELMPU is over. SELMPU also enables U6 pin 2 so that its output pin 3 can follow the state of the NWDS bus line (in the absence of SELMPU its output is permanently "Read"). Similarly it enables U6 input pin 13 so that the output pin 11, a signal called $\overline{\text{BUFFEN}}$ will go low, enabling the buffer in the presence of either of the strobes NWDS or NRDS (in the absence of SELMPU, $\overline{\text{BUFFEN}}$ is always high, i.e. the buffer is not enabled).

A signal DIR, which is the direction control for the data bus buffer on sheet 5 of the diagram, is derived from the NRDS line, on the basis that when the micropocessor is not reading it must be writing.

The duration of the monostable is made adjustable, so that it can be "fine-tuned" to suit the particular delays etc. present in the components on the card. It is very easy to adjust without special equipment since it simply needs adjusting for the minimum "snow" on the display. Maladjustment causes no problems other than an inferior

picture so it is not at all critical.

Sheet 4. 32-Character Counter, 10-Picture Line Counter, and 24-Row Counter.

These are fairly straightforward as their purpose has been extensively discussed in the Block Diagram description, and the source of the R and V signals has been discussed in the description of the circuit on Sheet 1 of the diagram. The 32-character counter outputs are C0-C4, the 10-picture line outputs are PL0-PL3, and the 24-row outputs are R0-R4.

However the layout of the signals C0-C5, and R0-R4 on the diagram needs some comment. This arrangement has been provided for the convenience of users who are wishing to experiment with 64-character lines. In order to count double the number of characters in the same time interval the input clock "0.75 MHz" must be doubled and an extra character counter line (C5) provided. If C5 is connected to the video RAM it will displace the first row-counter line R0, which in turn must be moved down to R1, which will have to move to R2, and so on, eventually R4 having no place to go; a result of the fact that only 16 lines of 64 characters will use up the whole 1K video RAM (64 x 16 =1K). If the original 24 lines are required, extra RAM must be added, to accommodate the displaced R4 row counter.

The circuit diagram reflects the actual track layout on the card, (for the symbolism see Sheet 8 of the circuit diagram), so as to ease the task of those users who are straying from the straight and narrow in wanting to alter the format of the VDU-K. By the way it is suggested that such users contact the user group "Interaktion" who will almost certainly be publishing hints and tips on this subject in their newsletter.

Sheet 5. Multiplexer, Video RAM, Buffer, Octal Latch.

The multiplexer comprises U16, 17, and 18, the control input in each case being the SELMPU signal. SELMPU is high when the microprocessor is executing a read or write of the video RAM (U26 and 27), and it causes the various "A" inputs of the Multiplexer to be switched over to the "B" inputs, which in the main connects the address bus AB0 to AB9 to the video RAM rather than the Character and Row counters C0-C3 and R0-R4. Thus SELMPU gives control of the video RAM over to the microprocessor, ready for a read or write. An extra line which comes out of the multiplexer is $\overline{CS}$ which has to be low to enable the RAM. Normally $\overline{CS}$ is connected to 0V via U18 pin 11, but this signal is obtained from U18 pin 10 i.e. $\overline{BUFFEN}$ when SELMPU is high. This is all shown on the timing diagram in Section 5, where it will be seen that in the case of a read $\overline{BUFFEN}$ is also 0V, so the video RAM remains selected, but in the case of a write $\overline{BUFFEN}$ is high for a little while before it goes low for the write. This short time is quite significant because it causes the outputs of the video RAM to go tri-state in anticipation of having data thrust upon them when the data bus buffer U19 is enabled in the direction for a write.

Had $\overline{CS}$ been wired to a signal which was permanently low no particular

change in operation would be observed, but there would be a bus "contention" when the buffer forced data onto the data lines of the RAM before they had time to go tristate for a write. The contention would only last for sixty nanoseconds or so, but while it did the +5V rail effectively would be short circuited to 0V, via the output drivers of the RAMs and buffers on each line which was in conflict. The 74LS645 is a very powerful driver so it would probably win over the RAMs, so it is likely that the RAMs would bear the brunt of the short circuits described. The 2114L RAM is however very robust and it is unlikely that failure would result. A more subtle problem could be the production of a large amount of system "noise" (spikes etc.) which could conceivably corrupt some data somewhere, trigger some latches and so on.

(A lot of fuss is being made over this point because it has to be considered if extensive modifications are made to the VDU-K card which result in alteration of the $\overline{CS}$ arrangements.)

The signals on pin 15 of the multiplexer I.C.s are wired low so as to enable the outputs permanently.

Note that U17 pins 5, 6, and 7 are spare, and can be used for any experimental purpose.

U19 has already been mentioned. It is enabled by the $\overline{BUFFEN}$ signal which goes low when SELMPU is high and there is either a read or write strobe present. The direction is controlled by a signal called DIR which is derived from the Read strobe from the Bus, on the basis that when the microprocessor access is a read it is a read, and when it is not a read then it must be a write.

The final IC on this sheet of the diagram is U25, the octal transparent latch. Normally its control pin 11 is high which renders it transparent i.e. the data on the inputs D flow through to the outputs Q, but the instant a microprocessor access begins the latch is rendered "opaque" or "frozen" by the low on pin 11. This action preserves the current data for the circuits which follow it, since these data would otherwise almost certainly be corrupted by the microprocessor access, causing "snow" on the screen. Since the $\overline{LATCH}$ signal is extended by the action of the monostable which produces it, the latch only becomes transparent again after the data from the video RAM have returned to valid values for the current character for display.

The internal labelling of U26, U27, and U25 deliberately does not distinguish the various inputs and outputs, so that for example the address lines shown within U26 are all marked "A", and the outputs are all marked "O". The reason for this is that they are all interchangeable, i.e. it doesn't matter at all at what physical location within the chip the data are stored, just so long as reading that same address will result in the same data being output (which of course they will on the basis of what goes in comes out). Similarly, the eight "D" inputs in U25 are in no particular order, as they represent eight interchangeable inputs, (but note that the "Q" outputs have to correspond directly to the appropriate "D" inputs, so that for

example output pin 12 is the Q output of the D input which is connected to the D input opposite it on this drawing, namely pin 13).

Sheet 6. Character Generator(s) and Dot Rate Shift Register.

This part of the circuit is the part which turns the data in the video RAM (generally held as an ASCII code) into the pattern of dots which will form the visual representation of that character on the screen.

As each character in the video RAM is held in the form of a single byte, and each character on the screen comprises a matrix of eighty dots (8 x 10), the central part of this circuit provides the means for a single byte input code to release the corresponding pattern of eighty dots.

Ignore for the moment LD7, and the circuit which is adjacent, and imagine that a (7-bit) ASCII code from the video RAM has been latched on the seven ("latched data") lines LD0 to LD6. Furthermore, increase the power of your imagination to assume that only U24, the "standard" character generator EPROM, is present, and U23, the "applications" EPROM, is not.

Suppose that the character to be displayed is some letter, say letter "A", which is represented by the ASCII code 41 (hexadecimal). This code is therefore present on the seven lines LD0-LD6 which contribute the high order lines (A4 to A10) of an address in the EPROM. The lower order address lines (A0 to A3) are contributed by the four lines from the "picture line counter", PL0 to PL3. The picture line counter, it will be remembered, starts at zero, and is advanced by one count at the end of each displayed picture line, until 10 complete lines have been displayed, at which point it goes back to zero again. The successive counts of the picture line counter access ten successive locations within the EPROM, and eight bits of data are output on lines D0 to D7 for each of the ten counts. This is all for the same single character to be displayed ("A" in our example), which explains how the single ASCII character from the video RAM is transformed into a pattern of 80 dots (8 x 10) on the screen.

In each of ten passes, eight dots are obtained from the character generator, which of course has been programmed with the appropriate pattern to produce the character in question. All 0's would be black, and all 1's would be white, but usually there will be a mixture of 0's and 1's, spaced out suitably to form a recognisable character.

The reason for using the dots eight at a time is mainly because common EPROMs have eight bits stored in each location, but it is very convenient to deal with eight at a time, since this means the accesses to the video RAM, EPROMs and so on can be relatively leisurely, which means in turn that readily available components can be used (i.e. not expensive high speed types).

As the pattern on the screen is displayed a single dot at a time, the eight dots from the character generator are loaded in parallel into a shift register (U22, type 74LS166), which has a single serial output. A synchronous shift register is used, the term synchronous meaning

that all of the actions in the shift register are governed exactly by the signal on its clock input pin 7, (in this case the 6.0 MHz "dot clock"). This is important because for certain characters on the screen (e.g. a fine "chequerboard" pattern of alternating black and white dots) any slight deviation from perfectly even timing, say when a new character was being loaded, would result in visible "joins" between what should be an unbroken display on the screen.

The $S/\overline{L}$ input U22 pin 15 is high for shifting, and low to load in a new character on the eight input lines connected to CD0-CD7. Pin 15 is made to go low, to load a new character, just after the last dot of the previous character is passing through the shift register. In a normal asynchronous shift register, loading would occur at once thus spoiling the timing of the previous dot, but in this type the action is delayed until the next clock edge, so that the timing of the last dot of a character is identical to that of those dots which went before. Of course when the register is being loaded it is not being shifted, so it might be thought that one dot might be lost, but in fact the first dot of the next character does not need shifting into position; when the register is being loaded the data from input line CD7 into DH (pin 14) automatically flow through to output QH (pin 13) to become the first dot of the next character, without the need to be shifted until the next clock pulse, by which time the $S/\overline{L}$ input pin 15 has returned high.

The two 3-i/p AND gates and the U4 pins 1, 2 inverter shown in the top right hand corner of the diagram decode the binary count signals "6.0 MHz, 3.0 MHz, 1.5 MHz, 0.75 MHz", so that the $S/\overline{L}$ signal is given at the correct moment during the timing of each character. The Timing Diagram given in Section 5 of the Manual shows how these signals are produced, including the one named "next character", which is discussed below. If you do refer to the timing Diagram, bear in mind that it is idealised - as the counters used are ripple counters (for reduced chip count and low cost), the various outputs do not all change simultaneously. At the 6 MHz dot clock frequency the propogation delays are not so big as to cause any difficulties, but for experimental use at a 12 MHz dot clock frequency the delays are great enough to cause a delay of around half a 12 MHz clock cycle - effectively inverting it on the Timing diagram. For this reason an inverter has to be put in the clock line when experimenting with the 12 MHz clock frequency.

The two 3-i/p AND gates and the U4 pins 1, 2 inverter also produce the signal shown as "next character", which marks the exact end of each character. This signal will be shown on the next sheet of the diagram (sheet 7), where it is used to ensure that signals which affect the characters, e.g. reverse video signals, and the "H" signal which defines the margins, are as exactly synchronised as possible with the characters. This prevents for example small "pieces" of characters from straying into the edge of the margins, which would spoil the presentation of the display. In older designs this effect was not a problem since the alphanumeric characters were located in the centre of a blank box, and it did not matter if the blank box strayed into the margin - it was invisible anyway. However, the VDU-K permits each character cell to be black or white including the whole cell, entirely

at the user's option, hence the need for attention to this point.

It will be difficult for the less experienced user to understand the point of all the discussion above, regarding the various possible imperfections, as he will imagine that all VDU designs are executed implicitly to the same standards as the VDU-K, which older users will know is by no means universally the case!

Assuming that the reader has some sort of grasp of the circuit so far discussed, we can move on to the signal LD7 which was disregarded before, and also the "applications" character generator U23.

As the video RAM stores eight bit data (latched as LD0-LD7), and the ASCII code is only 7-bits (LD0-LD6), the remaining signal LD7 is "spare". In this design it can be used for either of two purposes, selected by the user, permanently, or switchable.

The first purpose is simply to provide a complete repeat of all 128 characters so far available, but this time in "reverse video", so for example writing the ASCII code C1 (hex.) in the video RAM will result in a reverse video letter "A" being displayed, since C1 (hex.) is derived from 41 (hex.), the code for the normal letter "A", by setting its highest bit to 1.

The second purpose is to provide a totally new set of 128 characters, in addition to the first 128, making 256 in all. Depending on the application the second set of characters may include some letters (e.g. a reverse video letter "A" for code C1 hex. to give the same effect as before) and some new graphics characters, or of course the new characters can be entirely different, whatever the user wishes.

In summary, the eighth bit can be used for selecting one of two alternatives; the same characters as before, but in reverse video, or a totally new character set. It is desirable to be able to select these by a switch, according to the needs of the actual program being run at the time, and the VDU-K offers two alternatives for the implementation of this switch. The drawings at the top left of the diagram symbolise the physical arrangement on the board. The 8-pin DIL area can be fitted with a DPDT DIL (double-pole double-throw, dual-in line) switch, or fixed wire links. This is not the preferred arrangement because such a switch is very rare, and also the board has to be removed from the system to make the change. (The DPDT DIL switch mentioned is very difficult to obtain, and the more common type 2 x SPDT can be used instead, but this has the drawback that as the switches cannot be operated simultaneously it is mandatory to remove the power before changing the setting.)

The preferred arrangement is to use the two rows of pins, P1 and P2, to provide a connection area for a conventional DPDT switch mounted on the front panel, and fit nothing in the DIL socket. (This preference is of course only for general use of the board, with a front panel. If no front panel is fitted, and/or the switch is not required then the other arrangements will be found most useful.)

Whatever arrangement is made the circuit function is fairly

straightforward. A single line LD7 is an input to this part of the circuit, and there are two outputs; one to the first EPROM U24 via a link and the second EPROM U23 via inverter U4/3,4; another is a signal called REV (which stands for reverse video). LD7 is routed to one or other of these outputs and the other output, whichever it is, is earthed. In the REV position of the switch (marked on the diagram), LD7 is connected to REV, so that reverse video is under the control of LD7, and U23 (if fitted) is turned off, since its chip enable line pin 18 is driven high by the low on the input of the U4/3,4 inverter.

In the alternative switch position U23 pin 18 receives an inverted version of the LD7 signal, and is thus enabled whenever LD7 is high. REV this time is always low and no reverse video is applied (except of course for any reverse video characters which may be programmed into U23).

It has been assumed so far that the "EPROM type selection links" shown on the diagram are in the solid positions, and that 2K EPROMs type 2516 or 2716 are in use. In this case it can be seen that the two EPROM chip enable input pins 18 come from the same source, but inverted in the case of U23. Thus when U24 is "on", U23 is "off", and vice versa. This technique is in effect turning the two 2K EPROMS into a single 4K block, and nowadays single 4K EPROMs are readily available, so some users may prefer to use one of these instead. The various EPROMs available have similar pinouts, to a greater or lesser extent, according to their type and size.

One common 4K EPROM, the type 2532, is so similar in pinouts to the 2K types, that it can in this design (not always in other designs!) be fitted in place of the 2K type, with no circuit changes. If this is done, the 2532 device should be fitted in position U24, and U23 left vacant; The 2532 should be programmed with both sets of characters, the "standard" character set in the first 2K, the "applications" set in the second 2K.

The reasons no circuit changes are required for this substitution is that pin 18 on the 2532 conveniently is the extra address line (A11) which 4K EPROMs have, and the other pins (20, 21) can still be connected to 0V and +5V respectively although their function has changed.

Another common 4K EPROM is the type 2732. In principle this can be used to replace the two 2K types in the same way as discussed above, but sadly it is not quite so pin-compatible as all the others. When a 2732 is used it should be fitted in position U24, and U23 left vacant. It should be programmed as indicated for the 2532 described above. However, most importantly, the EPROM selection links should be altered from the solid positions to those shown dotted. The arrangement of links on pin area P5 has been carefully chosen so that the two settings required are symetrical; in one case the top two pairs of pins are connected, and in the other it is the bottom two. If some form of reversible connector is used to make the connection it can be arranged to convert the board from one type of EPROM to another simply by reversing the connector, or if a 2 by 2-pin jumper link arrangement is used it can be moved up or down by one position to make the change.

The reason for these changes being necessary in the case of the 2732 is that the A11 address line is on pin 21, not pin 18 as before, and pin 18 has to be connected to 0V. As in the case of the other types of EPROM the function of pin 20 also is changed, but it should still be connected to 0V as before.

Sheet 7. Synchronisation and UHF Modulator.

The description of this part of the circuit can begin in the top left hand corner of the diagram. U20 is a positive edge triggered dual type "D" flip-flop, the clock inputs in each case being triggered by the "next char." signal which was developed in the circuit shown on sheet 6 of the diagram. There are two signals which control the display of characters on the screen; "H" which defines the horizontal margins ("H" is low in the margins, high to display), and "REV" which is high if the current character is to be displayed in reverse video. for a "clean" display it is vital that these signals be synchronised exactly with the "next char." signal which defines the exact point of transition between one character and the next. The "Q" outputs U20/5,9 take up the levels of the "D" inputs (U20/2,12) in exact synchronism with the clock ("next char."). The purpose of C18 will be mentioned in a moment.

The U20/5 output (derived from the "H" signal input) enters AND gate U15/10,11 and so the U15 output pin 8 is unconditionally low when "H" is low (i.e.in the margins), and follows the U15 input pin 9 in the display area (where "H" is high). U15/9 comes from U12/8. (R10 is merely a pull-up resistor as U12 is an open collector device.) U12 is an EX-OR gate which has two inputs, pins 9 and 10. Pin 10 is a signal called "dots" which is the serial pattern of dots from the shift register, and pin 9 is derived from the "REV" signal, which is high if the current character is to be displayed in reverse video. The feature of the EX-OR gate which is used here is the fact that its output pin 8 will follow its input pin 10 when pin 9 is low (i.e. normal video), but its output will give an exactly inverted version of input pin 10 when pin 9 is high (i.e. reverse video).

The pattern of dots, inverted or not inverted as the case may be, passes through U15/9,8 under the margin control signal U15/10,11 already described. When the circuit was designed the reverse video feature was to be achieved by programming reverse video characters into the second EPROM, and it was only an afterthought to provide for this also in hardware by adding the U12/9,10,8 EX-OR gate. An unfortunate consequence of adding this additional feature is that the signal path from U20/9 to U15/9 is delayed by the EX-OR gate, when compared with the signal path from U20/5 to U15/10,11. C18 connected to U20/5,6 is a minor modification, which can be omitted at the discretion of the user, which slows down the signal transition to compenstate for the additional delay imposed by the EX-OR gate in the other signal path. Because C18 is connected between the complementary outputs U20/5,6 it will have a different effect on different edges (due to the unequal high and low drive capabilities of the 74LS series TTL devices used in logic circuits). This is a benefit because the tiny ghost dot-fraction which is to be removed from one end of the displayed picture line does not simply want moving to the other end of

the line, which would be the effect of a straight delay.

As always this is much ado about nothing, the imperfection which C18 is designed to remove is completely invisible to the average user. (If you want to search for it use the pixel block graphics at specific screen locations with the rest of the screen blank, and the brilliance control on your T.V./Monitor advanced to twice its normal setting - you may just see a faint vertical line in the join between picture area and blank margin.)

The signal which now contains the pattern of dots, correctly blanked in the top and bottom margins, is now taken through another EX-OR gate U21/9,10,8. The output signal called "vid", from U21/8 is exactly the same as the input U21/10 provided U21/9 is low, i.e. P4 pins 1 and 2 are connected together. If they are not connected R20 pulls U21 pin 9 high and U21/10,8 behaves like an inverter, i.e. the signal "vid" from pin 8 is the inverse of the input signal on pin 10. This effect is known as "Invert All" because not only all the characters, but the margins as well are inverted, i.e. "normal" video this time is black characters on a white background, just as on a conventional printed page, and any "reversed" characters appear as white characters overlaid on a character size black "box". Some advice is offered in Section 2 of this Manual on the subject of not being too quick to dismiss this setting, as in some applications some people prefer it. The designers' recommendation is to fit a SPST switch on the front panel (if fitted), so that all options are left entirely open.

There are two routes now for the "vid" signal; firstly (bottom left of diagram) to form a composite video output to drive a video monitor, and secondly (bottom right of diagram) to feed a high quality UHF Modulator which gives an output suitable for feeding a standard television receiver, via its aerial socket. As this latter circuit is the simpler to implement (all the complications being dealt with by the manufacturer of the UHF Modulator), this will be described first, after the following general remarks.

The two signals which are being brought together are "vid", which contains the pattern of dots required, suitably blanked in the margins, and "S" which is the combined line sync. and frame sync. signal used to synchronise the display device. As all of the timing is fundamentally under the control of the master crystal controlled Z80A-CPU-based Timing generator, it is possible to ensure that no sync. changes are present in the video display period and vice versa.

This makes the circuit to combine the "vid" and "S" signals quite simple, and in fact just two resistors are all that is required to provide the composite signal which is needed to drive the UHF Modulator UM1. The precise levels chosen suit the requirements of the modulator, and are set by choosing appropriate values for R12 and R13.

Space for two extra resistors (R11 and R14) is provided, but these are not normally fitted. They could be selected for example to give different levels to suit some other modulator, past, present, or future. Since R11 and R14 are connected to the d.c. supply rails they permit variations in the signal which cannot be achieved simply by

varying R12 and R13.

There will be some unit to unit variation in level because the signals depend on the voltage of an LS TTL logic "1", however the resistors have been chosen so that the modulator is driven by a signal which is larger than the minimum specified on the modulator data sheet so that it is sure to end up in the correct linear region of its characteristic in all circumstances.

The final part of the circuit to be described is shown at the bottom left of the diagram. The "vid" signal is buffered by U21/1,2,3 which is connected as a simple non-inverting buffer; similarly the "S" signal is buffered by U21/11,12,13 connected in the same way. In this case the buffers are not there in order to provide increased drive for the circuit which follows, instead they are there to ensure that the circuit which follows does not alter the levels of the circuit which precedes the buffers. This is important in the case of a card such as this which can drive both a t.v. receiver and a video monitor simultaneously; if alterations were made to say the video output components it would be far harder to get them right if they were driven from the same source as the modulator, because an alteration for one output might spoil the other.

Although U21 is not an open collector device, R15 and R19 have been provided to give a more accurate and defined logic "1", which takes some of the uncertainty out of the design of the rest of the circuit. The output U21/3 is reduced in amplitude by the potential divider formed by R16 and R17 so that it is a more suitable voltage for a video output to a monitor. The sync. output from U21/11 is shifted in level so that it swings below 0V, by the action of C15 and CR2. As C15 is a large (valued) capacitor it cannot charge or discharge quickly, and so its negative end (end 2) is forced to swing in amplitude to the same extent as its positive end (1). CR2 prevents end 2 of C15 from rising very much above 0V (this is called clamping) and so the sync. voltage applied as an input to end 2 of R18 is mostly a little over 0V, but falling a few volts minus when a sync. pulse is present. This causes a current to flow through R18 (and R16 and R17) and the resulting voltage dropped at ends 1 of the three resistors results in the sync. pulses being impressed onto what is now the composite video output. The three resistors can be juggled in value to alter the output if needed. This can be done by experiment, viewing the output on an oscilloscope, assuming it has a TVF trigger (for t.v. fields), or it makes a very interesting example of a calculation using Ohms' Law, Thevenin equivalent circuits and the like, for any academics who are members of our happy band.

The composite video output is deliberately not a.c. coupled since very high quality video monitors may keep the video path d.c. coupled throughout. (For the penalty which can result from not doing this see the part of Section 4 of this Manual which discusses a.c. coupling in video circuits.)

Sheet 8. Key to Symbols, and Power Supplies.

This hardly needs any explanation, so this part of the description can mercifully be fairly brief.

A Key to the various symbols used are described at the foot of the drawing.

All of the decoupling capacitors are shown on this drawing, although for electrical reasons they are distributed widely about the board.

This concludes the detailed circuit description.

3.1 CONSTRUCTIONAL NOTES

Introduction

As this card is supplied as a "bare board" as well as a kit, many users will be assembling it in a way which suits their own particular needs and wishes. Certain items (such as the UHF modulator, selection switches, front panels, video and UHF connectors) are omitted from the parts kit to follow the policy that only the basic most essential parts are supplied, to give individuals the chance to build their system as cheaply or expensively as they themselves wish. However to avoid permeating these constructional notes too much with mention of these options it will be tacitly assumed that the majority of all the options are to be fitted. Therefore if you find yourself being instructed to drill a hole for say a switch or video connector, which you haven't got, and don't want, then remember to ignore that section of these notes.

1. Read all documents very carefully before starting.

2. Do not remove the Static Sensitive devices (i.e. Z80A-CPU, 2716 etc EPROMs, 2114s) from their anti-static packaging at this stage. Identify all the components and using the Component Overlay, and the Parts List, work out where they all going to fit before soldering anything.

3. The "B" side of the board is the side which is visible when the card is viewed in the same way as is illustrated in the Component Overlay diagram, i.e. the diagram is drawn looking at the "B" side. The other side is the "A" side, and the components are (in the main) inserted from the "B" side and soldered on the "A" side, when the time comes. (Most issues of the card are marked somehow to aid in identification.)

4. Carry out any drilling or filing necessary to fit the card in the rack, to bolt on the front panel, and to suit the UHF Modulator if required. (This work should not be necessary, but if it was it would be a lot more difficult to carry out without the risk of damage once the card had been assembled.) In order to get the longest life from the edge connector sockets in the rack it is a good idea to chamfer lightly all of the edges of the card around the gold-plated area - but do not overdo this!

5. Check that there are no obvious defects on the board, e.g. damaged or short-circuited track etc. Look especially beneath the IC socket positions since they will be hidden in the finished job.

6. Consult the Component Overlay, and the Parts List, to determine what goes where. Any convenient order may be followed, but a typical method is to start with the lowest height components and work up.

   The following steps can be used as a check-list:

(a) Fit resistors R4, R5, R6, R9, R10, R12, R13, R15-20. (Note! Fit the correct values - the colour code is given in the Parts List.) They may be fitted either way round.

(b) Fit the diodes CR1-CR2. (Note! Fit them the right way round - see the Layout Diagram and the sketch on the Parts List. CR1 is the larger of the two diodes.)

(c) Fit IC sockets for S1-2 and U1-U27. Be sure to use an acceptable type of socket if you are going to take advantage of the board supplier's fault-finding service - see the Fault Finding Section of this Manual for further remarks on this subject. Make the identifying mark on the socket correspond to the Pin 1 end of the DIL switch or IC. Do not plug any components into their sockets yet.

(d) Fit RV1.

(e) Fit C1-17. (Note! C11, C15, C17, are polarised types which must be fitted the correct way round. The "+" lead of the capacitor will be marked "+", or can be identified by a process of elimination as being the lead which is not marked "-".) Consult the sketches in the right-hand column of the Parts List (at the back of this Manual) for further guidance. Go through the whole list of capacitors, comparing the different types and quantities supplied, if you are not used to capacitor markings, until you are sure you know which is which.

(f) Fit R1-3 and R7-8. (Note! Fit the correct values - the colour code is given in the Parts List.) As these resistors are mounted "on end", care must be taken not to strain them where the wire leads enter the resistor body, when the wire leads are bent during installation. Hold the wire to be bent with pointed pliers close to the resistor body and make the bend on the free end of the wire. Some of the resistors are "pull-ups" and if they are damaged they will not necessarily stop the computer from working in the early stages, but they may cause trouble much later, perhaps when extra cards are added, and you will forget to look on this card for a fault, because it will have been working for so long.

Note that R1 and R2 are best mounted exactly as shown on the Component Overlay diagram, i.e. with the body of the resistor towards the crystal Y1. If they are mounted with the body away from Y1 there is a risk that the crystal could be pushed into the wires of the resistors shorting them together if the crystal does not have an insulated metal can.

(g) Fit Q1. (Note! Q1 must be fitted the correct way round, see the b,c,e lead identification markings on the card, and the drawing overleaf.) Do not pull the leads too tightly.

Top View (leads away from you)

Note that this diagram does not follow the convention given on transistor data sheets, i.e. giving an under-view. Instead it follows the convention given on IC data sheets which generally show top views.

(h) Fit the five 0.1" pitch pin assemblies P1-P5 (two 2-pin, two 3-pin, and one 5-pin). Pass the short length of the pins thorough the card from the top and solder on the underside, like all the other components.

(i) Fit the 9-pin 0.1" socket strip which is used as a socket for SIL 1. One type of socket strip which may be supplied is just like half a dual in line (DIL) integrated circuit socket, and is fitted to the board in the same way as such a socket.

The other kind of socket strip comprises a number of formed sockets on a one-piece carrier. Do not break off the carrier yet! Solder the strip in position and when you are sure everything is correct, and only when, break off the carrier by bending it gently back and forth with long nosed pliers, being certain not to distort the socket part in any way.

(j) The quartz crystal Y1 has been left to this late stage because it is susceptible to mechanical damage, and should only be "at risk" for the shortest time. It is mounted vertically. The frequency is usually marked on the body of the crystal, and is given in either kHz or MHz. The crystal leads should be inserted in the appropriate holes in the circuit board; it is not a polarised component, and can be fitted either way round. Solder the crystal in place. (Note! The crystal is sensitive to overheating when soldering.)

7. Install any DIL switches which are to be used, and SIL 1. (Note! Be sure to get the switches right way round if it matters, and note that SIL1 must be fitted right way round; pin 1 of the SIL Resistor pack will be identified in some way.)

8. If you wish, use a suitable solvent to remove any flux deposits from the track side of the board. (Note! Some solvents also dissolve some types of plastic.) Also note that over-zealous use of flux-removing solvents can actually cause trouble, by washing impurities into connectors and IC sockets. You can give some protection by covering them with masking tape, but in many cases it is better to ignore this step altogether.

9. If a metal front panel is to be fitted (which is recommended) drill the holes which you are going to use in your own particular

application, according to the drawing provided in the Diagrams Section of this Manual. (Note! Take care to avoid scratching the metal card front).

10. Fasten all of the front panel components to the panel, except the front handle. The drawings show the general arrangement of the front panel components, but of course these can be varied to suit individual needs and choice.

    When fastening the TV aerial socket to the front panel use two M2.5 x 10mm pan-head screws. Fit a nut with a serrated washer to the right hand bolt (viewed with the panel upright, with the aerial socket towards you). The serrated washer is fitted immediately below the nut. On the left-hand bolt fit two serrated washers, with a solder tag between them. Note that it is a most important step to fit the serrated washers on the left-hand bolt exactly as described; in order to reduce interference patterns on the the t.v. display the screening has to be complete. The aluminium front panels are supplied with a surface which is a poor conductor, and the first serrated washer is used to bite through this surface to give the necessary connection between solder tag and panel.

11. Solder a 30mm length of tinned copper wire to the centre pin of the J1 front panel TV Aerial socket, and slide on a precut length (20 mm) of 1.5 mm diameter silicone rubber sleeving.

12. Turn your attention now to the modulator. Fit the extension screening piece (10mm dia tube) to the output (UHF) socket of the modulator. The end of the screening extension which is slotted is the end which should be fitted to the modulator. It should be a tight push fit; take care to hold the modulator so that only its case takes the stress of fitting the extension piece. Push the extension piece on just far enough to enable the front panel to be fitted next in its correct position. Insert the modulator in position on the card, bend its two earth tags slightly and solder in position. Solder the two connections to the modulator.

13. Carefully prise the lid (i.e. the side with a label) off the UHF Modulator. Do not touch any of the internal modulator components as this may disturb the tuning (at UHF, Ultra High Frequency, what may look like a loose bit of wire is in fact part of a tuned circuit, so leave everything strictly alone!).

14. Pass the sleeved wire from the front panel socket inside the extension piece and through into the modulator interior. Fasten the front panel to the card using the special plastic mounting brackets and the nuts and bolts provided for the purpose. Fit the front handle, and front panel screws. Solder the wire inside the modulator, remembering to touch nothing else within, and replace its lid. Connect the nearer of the earth tabs on the modulator case to the front panel solder tag using a short length of tinned copper wire.

15. Connect all the front panel components used (switches,

connectors) to the appropriate places on the board. Wire-wrapping is a recommended method, or push on crimped connectors, or even, if you have no alternative, soldered to the pin assemblies.

16. Connect C18 as neatly and tidily as possible on the track side of the board between pins 5 and 6 of U20. This is not an important component (its purpose is discussed in the detailed circuit description of sheet 7 of the diagram - see Section 2.4 of this Manual), and its installation may be postponed if desired.

17. If desired the board may be laquered on the underside. A suitable printed circuit board laquer should be used, and similar precautions should be taken as described in the earlier paragraph (no. 8), to prevent the connectors and IC sockets from becoming contaminated. It is probably safest to ignore this step if you are in any doubt, as a lot of damage can be done through lack of experience here. (Note! Be sure not to laquer the gold-plated edge connector on the card.)

This concludes the constructional notes. The next section of the Manual covers testing and setting up.

3.2 TESTING AND SETTING UP

1. Check that all components fitted so far are in the correct place, and have the correct polarity where appropriate. Re-read the constructional notes - important points are prreceded by the loud word "Note!", and can be checked again now.

2. Inspect the board for dry joints, solder bridges an solder splashes, paying particular attention to areas where tracks run between IC pins. Shine a strong light through the board, and use a magnifying glass if you have one.

3. Apply power to the board and check +5V supply at all the IC positions where this voltage is used, i.e. the corner pins of the ICs excepting IC1. If you consider you are likely to cause damage by carrying out this test, or are very confident of your workmanship then omit this step at your own discretion.

4. Remove the power, and wait for the capacitors to discharge (if necessary use a few hundred ohm resistor to discharge them more quickly), and insert all ICs the correct way round. Note the remarks on handling MOS devices, given in Section 1 of this Manual.

   Usually the ICs are supplied with their leads slightly "splayed" - don't just shove them into their sockets without using the greatest care. An IC insertion tool will hold the leads parallel at the right spacing; if you don't have such a tool, bend the leads slightly at their "shoulder", on a flat surface, (which should be conductive for the MOS devices). The sockets supplied in complete kits have been specially selected for their ability to provide high reliability connections, but the foregoing warnings are intensified if you are using your own sockets instead. There are some remarks in the Fault-finding Section later on the subject of difficulties which have been met with certain types of IC sockets, so study this before proceeding if you are in any doubt.

5. Important! Re-check the orientation and position of all ICs, as an error can have disastrous consequences. As it is hard to check your own work, preferably get someone else to check it for you.

6. Make sure that the correct links have been made on P5 to suit the type of I.C.(s) used for U23 and U24.

7. Set S2 (or the links which replace it) to a suitable address for the software in your system. If this is Interak 1 running ZYMON 2 the address will be F000 (hex.).

   The various switch etc. settings are discussed in Section 2.3 of this Manual.

8. If you have any suitable contact lubricant apply a small quantity to the gold plated edge connector. This will greatly reduce wear on the gold plating and the bus sockets. An alternative type of lubricant which has been used with no apparent ill effects is a branded product "WD-40", however as it has extremely penetrating properties it should be used most sparingly to prevent the very real risk of lifting the gold-plated copper tracks and rendering the card useless. Fit the card in such a position that you can adjust RV1 without removing the card, or use an extender card if you have one.

9. It has to be assumed at this stage that you have a working system with fully tested cards, but of course if this card is the only VDU you have this will obviously not be the case. In such circumstances you will have to bring the system up to correct operation as best you can, perhaps seeking advice and reassurance from the card supplier, or perhaps "Interaktion", the users' group for the Interak computer.

10. Connect the T.V. receiver or monitor, switch the system on and hope that you receive your first message from the computer. (In the case of ZYMON 2 this will be a clear screen and the title near the bottom "ZYMON 2", its version number, and an invitation to "ENTER COMMAND".)

11. If you are not at the stage of having a working computer complete with operating software, then you can still try out the VDU-K. If it is installed virtually on its own then a complete screen display of random characters should be obtained. In many cases this is more attractive than the blank screen referred to earlier, since there will be an interesting variety of characters displayed, in both normal and reverse video.

12. It may be the case that no picture is displayed at all. If anything untoward is noticed (such as sizzling noises, or dense black smoke - no laughing matter) then switch off immediately and refer to the Fault Finding Section. Otherwise leave the power on and try some further procedures. Check carefully (by hand) for any overheating chips, which needless to say is a bad sign, but if they feel fairly cool try the following:

13. If a T.V. receiver is in use, ensure that it is correctly tuned to suit the UHF Modulator. The correct channel is channel E36, but beware that the calibration of T.V. tuning dials is often quite inaccurate. Although normal operation is to have the sound turned off, turn it up a little while you are trying to tune the set. A sharp buzzing sound is a good sign that tuning is near, but plain background hiss is not. At this stage a picture that is all black or all white is better than nothing, but ideally it should show some recognisable characters. If you can get no picture at all, then refer to the Fault Finding Section, which is all you can do if you get a picture which does not show any characters, or which will not synchronise, or has incorrectly displayed margins etc. etc.

14. Once you have a picture you can check the card out generally. It is suggested that a random display of characters be produced, under computer control if you have it, or by having no CPU, or by switching the S2 addresses to some unused area in your system memory map.

15. If you have a front panel Rev/Alt switch this can be used to switch in the alternate character generator EPROM. If no such EPROM has been fitted then its selection should cause about half of the random characters on the screen to go all white (since an empty socket is equivalent to a set of characters full of dots). Do not worry if any of these white characters are a little ragged, this is because the logic levels concerned are floating up to a logic 1 rather than being driven firmly. (This will effectively confound those "experts" who say an open circuit TTL input is a reliable logic 1; it isn't when there's some fast signals around!)

    If you do not have an alternate character set EPROM to plug in position U23 you can use an EPROM programmed with any data, even a machine code program. It is very unlikely to produce recognisable pictures, but there might be a fair chance of success if you were to use it to apply for an Arts Council Grant for your services to Modern Art.

16. Check (if a suitably programmed timing EPROM U2 has been fitted) that you get a non-interlaced and an interlaced display when the lowest switch in the S2 pack is altered. See Section 4.5 of this Manual for an explanation of the difference. Choose the one which suits you best, and don't be surprised if it turns out to be non-interlaced.

17. The final simple check is to open and close the connection between pins 1 and 2 of pin assembly P4. This should cause the whole screen to be alternately inverse video and normal video. Do not be alarmed if the brightness and contrast controls of your display device need readjusting for these two settings. This is quite normal for a display device which does not have a feature known as "black level clamping", and it is a subject which is discussed further in Section 4.6 of this Manual.

18. Finally there is one adjustment to make to the VDU-K card, assuming it has passed all the above tests. This is to find the best setting for RV1. This cannot be done unless the VDU-K is used as part of a computer, having preferably a Z80A-CPU running at 4.0 MHz with no wait states in the video RAM area.

    Two small test programs are given next, one in the ZYBASIC language, and one in machine code. They serve the same function, namely that of repeatedly accessing the video RAM while the video is using it. The ZYBASIC program is probably the more stringent, as most versions of ZYBASIC use the Block Move instruction which is the one with which it is most difficult to cope. Of course there is no reason why a more complicated machine code program could not be written utilising the block move instruction within

the video RAM, for the benefits of those unkind people who like to see a VDU-K suffer.

It is assumed in the machine code program that the VDU-K Video RAM is located starting at address F000H.

ZYBASIC VDUK Setting-up Program.

```
10   SCROLL: PRINT "Hello": GOTO 10
```

Machine-code Setting up Program.

```
0800 3A00F0     START:    LD A,(F000) ;Access the VDU
0803 18FB                 JR START    ;And again and again
```

Once the program (whichever you use, preferably try both) is running adjust RV1 until a snow-free display is achieved, if this occurs over a range then set RV1 in the middle of that range. If an oscilloscope is available confirm that the monostable pulse (measured at U3 pin 8) is approximately 640ns at the optimum setting.

For Amusement Only

The Z80A-CPU timing is most stringent when it is executing an op-code fetch ("M1 Cycle"). Even with the 200ns type of RAM used, the access time of the video RAM is too long to guarantee operation for an op-code fetch in the video RAM, but if you have a fair wind behind you may just be able to use it to run an executable program in the video RAM itself, e.g.

```
F200 18FE    MAYBE:    JR MAYBE  ; That's it - looks easy but
                                 ; it's not!
```

It takes some ingenuity to get a program into the video RAM (Suggestion: use ZYMON to fill F000 onwards with 00 (NOP), then just copy in the two bytes of the program from somewhere else - use ZYMON's COPY command. You can then execute at F000 and just trickle through the NOPs until you hit 18FE). Adjust RV1 as before. If you succeed in running this program, and if you have the facilities, try adding some wait states, or dropping the clock frequency to 2.0 MHz, and see what a mess there would have been on the screen without the anti-snow feature!

19. To examine the character set on the screen you can use a variation of the example program given in the ZYMON Manual, or the following ZYBASIC program:

```
10   FOR J = #F000 TO #F1FF
20   POKE J,J
30   NEXT J
```

20. Try filling the video RAM with various data, and make sure all the characters are the same, especially when they are scrolled up, e.g. by ZYMON or ZYBASIC. If they are corrupted when you are working with the card on an extender do not be alarmed, however this should not happen when the card is plugged into the rack. If it does, see the Fault Finding Section.

This concludes testing and setting up. The next section of the Manual covers fault finding, and return for service.

3.3 FAULT FINDING, RETURN FOR SERVICE

As a fault will be the result of any one or more of hundreds of possible things going wrong (he said cheerfully) it is of course not practicable to give any more than a guide to the location and correction of faults, but the procedures below will at least give some idea of how an attempt at fault-finding can be made.

Experience with other cards has shown that the major cause of faults in cards assembled from kits is due to soldering errors (e.g. "dry" or unsoldered joints, and bridged tracks). The next most likely cause is the setting up of the DIL switch options, then comes misplaced components and even obvious mistakes like missing ICs or ones plugged in upside-down. In the case of "bare boards", other common causes of faults are incorrect component substitutions (the user can't see any reason why he can't use some other component to that specified, but the VDU-K card can!), and mis-insertion of i.c.s into their sockets; we shall have a great deal more to say on this latter subject later.

It is very rare for an IC to be supplied faulty (each one has to be tested and characterised by the manufacturer as part of the manuacturing process), and this is borne out by the fact that "ready made" Interak Cards very rarely suffer defective chips; faults found on test are invariably due to some other cause.

However, all the time a board is being tested it is "at risk" (ICs are being pulled in and out, voltmeter and test probes are being prodded about and may short pins of ICs and pcb tracks together). It is frighteningly true that if you test a good board often enough you will eventually cause a fault!

When reading the following procedures remember that they are only suggestions, and there are plenty of other faults which often cause misleading symptoms.

If an oscilloscope is available some waveforms can be measured on the VDU-K card if is suspected this is at fault. Some places to look are given later in this section.

Many professional users will be in a position to find any faults without undue difficulty, and will therefore want to do their own fault-finding should the need arise. Other less experienced users will wish to do the same, but this time on the grounds that there is no better method of gaining a real understanding of computer hardware than tracing faults and fixing them themselves.

However laudable as these two aims may be, the company who supplied the kit will be prepared to help any of their customers who are in difficulties. The charge will probably be very little more than the cost of return postage and any parts which have been damaged.

There is no shame in admitting defeat - some tricky faults can baffle even the most experienced expert, and in many cases advanced test equipment will be needed which will just not be available to the

average user.

If it is necessary to send a circuit board through the post, make sure the recipient knows to expect it. When making arrangements for the return of a board, be ready to quote the number of the invoice on which it was supplied, or approximate date of purchase. (A supplier will understandably not be so keen to help if the kit was purchased from someone else!).

For transit through the post, pack the board(s) well, wrapped in e.g. aluminium cooking foil for anti-static protection, and remember to include your name and address, and payment e.g. by means of an ACCESS or VISA card. A suitable postal service should be used both ways, e.g. Registered Post, Recorded Delivery, or Compensation Fee Parcel Post, even though this does cost more.

Warning.

There is a great art to replacing components and working in general on a plated-through hole board, and high quality, expensive special tools are needed, and the skill and experience of people who have spent many long years learning their craft.

Having seen the results of some peoples' efforts we urge you to do anything other than try to unsolder an IC socket from a through-hole plated card. Cut tracks, plug the IC in with one lead bent out of the socket, and wire-wrap the missing connection onto the leg of the IC, anything! If you do have to remove a socket then don't try to salvage it. Smash it to pieces, and using tweezers remove the pins one by one, applying the minimum of heat and force to avoid pulling them out complete with the plated through holes. (The possibility of this activity being enjoined explains why it is not recommended that the very expensive turned pin in solid plastic type of socket be used. If the socket cannot be broken into pieces for removal then there is a severe risk of damage to the card when trying to desolder all leads of the IC at once.)

The same goes for discrete components. To remove a resistor, chop it in two; a new one is only a few pence and it will cost several hundred times that figure to buy a replacement for a damaged board.

Some General Fault-finding Procedures.

The great difficulty in suggesting fault-finding procedures, is that the methods vary so much according to what equipment you have and your skill, knowledge and experience.

As the VDU-K is often one of the "essential" cards in a system, i.e. without it the system cannot be used, it is very difficult to be sure that any fault in the system is in fact located in the VDU-K card. Almost anything going wrong with any part of the system can cause something to happen to the display.

In many ways however the VDU-K is one of the easier cards to test. In a manner of speaking it can stand alone. Although it will then be

able only to display a random assortment of unchanging characters it takes a good deal of the circuit on the card to perform even this simple task, and so if you see anything at all there isn't likely to be much wrong.

In the event of any trouble do switch off and re-examine the card, checking quickly for any overheating. If an integrated circuit is inserted wrong way up it will often cause a heavy burden on the power supply (which fortunately is well protected internally if it is one of the recommended switch-mode types, and so should not suffer any damage). If the load is so great that it lowers the voltage on any of the supply rails then this could easily stop the computer working. It is almost certain that the heavy currents would cause the integrated circuit to overheat, in an extreme case causing smoke to come from it, and perhaps a minor explosion. Incredibly, integrated circuits subjected to such abuse can often still be fully functional when they are re-inserted correctly, but you are advised to replace them as soon as you can, rather than leave a potential source of weakness in the computer.

Experience shows that there is quite a good chance that there will be some visible physical fault, e.g. solder splashes on the tracks, unsoldered or "dry" joints, incorrectly inserted ICs, and so on, (e.g. ICs in the wrong sockets, or inserted badly, so that a pin is bent and makes a poor contact).

The integrated circuit sockets used in the kits are a high reliability type which has been most carefully selected after considerable experience. They have a tenacious grip on the ICs; it is also easy to enter the IC leads into the type of socket supplied, because of the lead-in ramp, and the generous and visible contact area.

Bare board users who have used some of the inferior types of socket widely available, must take special care to insert the ICs correctly, and should remember the sockets can be the cause of faults. (The "inferior" type of socket has a very flimsy contact and weak grip on the IC leads, and has the contacts hidden behind small "windows" through which the IC leads must pass. It is vital with such a socket to ensure that the IC is inserted so that the leads are true and straight so that they do not slip to the wrong side of the contact, or bend the contacts out of line - an IC insertion tool should really be used.)

Fault Finding Techniques.

The main requirement in successful fault finding is a thorough knowledge of the whole card and the way it operates. Once you have this (and it is hoped you will have if you have studied this Manual so far) you will be able to localise the fault to a particular area of the circuit, and then "home in" on the particular source of the trouble. For example if a perfectly stabilised and steady display was obtained, but the fault was that no reverse video characters could be displayed it would be fairly pointless to start looking at the timing generator and counting chains, because they must be working fairly well to display any kind of stable picture. In such a case a

sensible place to start looking would be the circuit which controls the selection of reverse video characters, the most significant bit from the RAM, the Alt/Rev selection switch and so on.

On the other hand, if the fault was a very weak, grey picture, it would be foolish to start looking for trouble in say the data bus transceiver or the address decoder, whether the data are good bad or indifferent they should still be displayed perfectly.

Description of Circuit from the Point of View of Fault Finding.

The circuit has already been described at length, in various degrees of detail, in Section 2 of this Manual, but it is proposed to take another pass through the diagrams, this time from the point of view of looking for various things which can be considered when fault finding.

Sheet 1. The Block Diagram.

With the exception of printing mistakes there is not much to go wrong here, but it is recommended that this be studied first when fault finding so that a "battle plan" can be formulated. Ask yourself where could the fault be to explain the symptoms you are suffering. For example if you are getting characters displayed in the margins, where they should be invisible, could it be the crystal oscillator at fault? Not really - if that wasn't working there wouldn't be a picture at all. Could it be the UHF Modulator? Again, not really, if it was being incorrectly driven it wouldn't display anything, certainly it is inconceivable that it could be generating characters of its own in the margin. By asking questions like this it should be possible to deduce from the block diagram alone, the general area of the fault, and you can then move on to study the chosen part of the circuit in depth.

Sheet 2. Oscillator, Dividers, and Sync. Generator.

Is the crystal oscillator oscillating at 12 MHz? (Probe at U8 pin 6 rather than the crystal circuit itself to avoid disturbing its operating conditions and possibly stopping it yourself.) Are there the various binary divisions in the outputs from U14? If not, are the reset pins (U14/2,12) jammed high? Pin 2 should be always low, pin 12 should have the waveform shown in the appropriate diagram in Section 5 of this Manual. Is the Z80A-CPU receiving a full swing clock signal of the correct frequency? If not is the active pull up, Q1, working correctly? Is it connected right way round? Has some one substituted a different transistor? Is it PNP? With the correct pinouts (b,c,e)? Have the right value resistors been used? 22R not mixed up with 220R?

If the clock is O.K. is the Z80A-CPU working? Look at U1 pin 27, the M1 line. There should be plenty of activity here if it is executing instructions. If not make sure it isn't permanently being held reset. U1/26 should be high. If not, why not? Is C11 correct polarity, not holding the line down low? Are U1/16,17,24,25 all high?

If the trouble is to do with the sync. pulses (i.e. you are getting a picture but it is not stable, or it is "torn"), is the "S" signal (U13 pin 2) correct, see timing diagram? If not, is it the timing program?

Check for read and write pulses on U1/21,22. Is there activity on the TA0-TA8 address lines? Do any signals look so similar that they could be short circuited? Ditto the TD0-TD7 data lines? Are the 0V and +5V connections to U2 (and the rest) all present? Probe the actual pins of the IC, remember it could be badly inserted into its socket. See if closing S2h has any effect.

Sheet 3. Address Comparator and Control Logic.

This is most difficult to test in a non working system as it is impossible to set up and run any test programs. If you are really desperate and you are sure your fault is here you can set up some static tests, e.g. hardwire the AB10-AB15 lines to some chosen address, NRFSH high, and NMREQ low, to see if you can get a match with the DIL switch S2 setting. Are you doing something silly, like setting the switches on when they should be off and vice versa? Are you setting them back to front, i.e. most significant digit confused with least significant? Is SIL1 plugged in right way round, are you sure pin 1 is pin 1? Fortunately, there is one part of the circuit which will hardly affect the operation of the card if it is faulty, and that is the monostable, U3. This is used purely for the anti-snow feature, which is a cosmetic improvement, the board will otherwise work perfectly well without it, assuming nothing drastic like the output stuck permanently high.

It is quite difficult to test this part of the circuit under the high speed conditions under which a computer operates, especially when as is likely to be the case if you are having trouble with this part of the circuit, the computer is not operating. Any small error will throw the whole logic out of operation, and without great experience and/or sophisticated equipment it is really only a matter of luck to be able to find a fault here. To give luck a chance, you can probe the various elements of the circuit - although the various waveforms encountered generally will be meaningless, you can look for lines which are "stuck" at "0" or "1", or which don't appear to be reaching a low enough "0", or a high enough "1", inverters which don't seem to be inverting, and so on.

It may be helpful to read through the Detailed Circuit Description earlier in this Manual, and to study the waveforms both on paper, and physically on the Card. As you gain an understanding of how the circuit operates you will be able to direct your own test procedures so as to find which piece of the circuit is malfunctioning, which is the first step to repairing it.

It is stressed again that if you do not have success in finding a fault that is present, you can always hand it over to someone else. The after sales service which is available to purchasers of the kits is one of the many things which mark out the Interak 1 System as being a unique and worth-while product.

Sheet 4. Counters.

In contrast, this part of the circuit is very easy to test, in that it is a very simple counter chain. For all the counters on this sheet of the diagram it is a simple matter of checking if there is an input, if so, is there an output, and so on for all the outputs? If there isn't an output, or if it isn't the correct frequency, then find out if the supply voltages are connected (to the actual pins of the ICs, not just the sockets). Are the reset pins jammed to the wrong logic state? Are they shorting to some other line, causing premature resets?

Sheet 5. Multiplexer, Video RAM, Buffer, Octal Latch.

This is another of the more difficult parts to test when the computer is not working. If the fault is in a lack of picture of steady well defined (but random) characters, then check pin 1 of the multiplexers U16 to U18. Mostly (in fact all the time if nothing is reading or writing to the video RAM) pin 1 should be low. This selects the cycle of counts on the "A" inputs (pins 2, 5, 11, 14), and transfers them unaltered to the "Y" outputs (pins 4, 7 ,9, 12). Check that it does. Be sure the $\overline{CS}$ line on the RAMs (U26/8 and U27/8) is low, and if it is check the ouputs (pins 11, 12, 13, 14) for some sort of activity. If they seem to be very low in amplitude see if they are in some sort of contention with U19, which could be caused if U19/1,19 were both low.

When nothing is accessing the card the outputs of the latch U25 should follow the inputs. If they don't, see that U25/11 is high, and U25/1 is low. If the latch was jammed to some particular character that character would be displayed on the whole screen, but often this symptom is the result of a runaway program writing the same data throughout the RAM, including the video RAM.

If a display of random characters is being obtained but it is not possible to change it then (assuming the rest of the computer system is free from faults) the fault could quite likely be in the multiplexers or buffer, or of course in the signal which control them. A very obvious cause of this difficulty is the lack of a write pulse for one reason or another, but you also have to be sure that the control pin 1 of the multiplexers is being activated, and the control pins of the octal tranceiver i.e. U19/1,19.

Sheet 6. Character Generators and Dot Rate Shift Register.

This is perhaps in the "easier" category. Problems associated with bit LD7 (reverse video which won't reverse, or an alternate character set which can't be obtained) should be fairly easy to find by tracing the circuit from LD7 through the links and/or switches. Is inverter U4/3,4 working? Are the character generators plugged in correctly, correct type selected on P5?

If recognisable characters are not being displayed are LD0-LD6 active? Are PL0-PL3 cycling round a count of 10 correctly? Are the outputs CD0-CD7 jammed for some reason? Or perhaps just one bit? (Pretty obvious from the display.)

Is the shift register U22 working, clocking out dots? Are the waveforms in the circuit just above the shift register basically correct (see Timing Diagram in Section 5.2 of this Manual)?

Sheet 7. Synchronisation and UHF Modulator.

Another fairly easy circuit to search for faults. For lack of picture content on a well stabilised display trace back from the line marked "VID". Just follow back through the inputs of the gates, until you see where the signal has come to grief. Checking the two flip-flops (contained in U20) is easy enough. If an output is wrong, then is there a clock input? If there is, are there data ("D") inputs of the correct polarity? If not, why not?

If the fault is a picture of sorts, which cannot be sysnchronised then check the line marked "S". Are the combining circuits which bring together the video and sync. information working, for either or both the video monitor output and the drive to the UHF modulator. Is CR2 the correct way round? Has it been snapped by clumsy bending of the leads? Are the resistor values correct?

Beginners, don't make the mistake of assuming that the UHF Modulator is faulty if you can't see any activity on an oscilloscope connected to its TV aerial output - you're not likely to unless you've got a very special oscilloscope! Is the case of the modulator earthed, via its earth tags, and is this connected to the front panel TV aerial socket?

Sheet 8. Key to Symbols, and Power Supplies.

There is not much on this sheet to go wrong, and it is a bit late in the day now to be checking if the power is connected, but if you have the world's most classic fault, a short circuited supply rail, then you will have to look at at all of the various decoupling capacitors shown on this diagram to see if they've got anything to do with it. Probably it is best to pull out all of the ICs just to be sure, but then it is a matter of cutting tracks, drilling out plated through holes and so on until you can find the faulty section of track. Better still send it back to the firm who supplied it, they were daft enough to volunteer to fix any fault you can put into a board, call their bluff!

This concludes the section on fault finding so the authors of this Manual hope the card is fixed by now, because they've run out of ideas!

4.1 Appendix 1: Standard Character Set Ref. CG02.XX

This characters shown on this page and the page following are an example of one set of characters that has been defined as a standard character generator set. They are largely based on the printable ASCII characters, but characters have also been allocated to the non-printable codes, such as carriage return, line feed, etc. Some further points to note are given at the end of the table on the next page. Purchasers of the VDU-K card as a "bare board" can obtain a pre-programmed character generator EPROM from their supplier at modest cost.

Hex.	ASCII	Displays		Hex.	ASCII	Displays	
00	NUL	□	Graphics Space	20	SP	□	ASCII Space
01	SOH	▘	Block Graphics	21	!	!	
02	STX	▝	Block Graphics	22	"	"	
03	ETX	▀	Block Graphics	23	#	#	
04	EOT	▖	Block Graphics	24	$	$	
05	ENQ	▌	Block Graphics	25	%	%	
06	ACK	▞	Block Graphics	26	&	&	
07	BEL	▛	Block Graphics	27	'	'	
08	BS	▗	Block Graphics	28	(	(	
09	HT	▚	Block Graphics	29	)	)	
0A	LF	▜	Block Graphics	2A	*	*	
0B	VT	▄	Block Graphics	2B	+	+	
0C	FF	▟	Block Graphics	2C	,	,	
0D	CR	▐	Block Graphics	2D	-	-	
0E	SO	▙	Block Graphics	2E	.	.	
0F	SI	▟	Block Graphics	2F	/	/	
10	DLE	┘	Line Drawing Char.	30	0	0	
11	DC1	└	Line Drawing Char.	31	1	1	
12	DC2	┐	Line Drawing Char.	32	2	2	
13	DC3	┌	Line Drawing Char.	33	3	3	
14	DC4	┤	Line Drawing Char.	34	4	4	
15	NAK	├	Line Drawing Char.	35	5	5	
16	SYN	┴	Line Drawing Char.	36	6	6	
17	ETB	┬	Line Drawing Char.	37	7	7	
18	CAN	│	Line Drawing Char.	38	8	8	
19	EM	─	Line Drawing Char.	39	9	9	
1A	SUB	┼	Line Drawing Char.	3A	:	:	
1B	ESC	☠	Alien 0	3B	;	;	
1C	FS	☺	Alien 1	3C	<	<	
1D	GS	☻	Alien 2	3D	=	=	
1E	RS	◄	Vehicle L.H.	3E	>	>	
1F	US	►	Vehicle R.H.	3F	?	?	

The remainder of the table (codes 40H to 7FH) is on the next page.

(Appendix 1 continued)

Hex.	ASCII	Displays	Hex.	ASCII	Displays
40	@	@	60	`	£
41	A	A	61	a	a
42	B	B	62	b	b
43	C	C	63	c	c
44	D	D	64	d	d
45	E	E	65	e	e
46	F	F	66	f	f
47	G	G	67	g	g
48	H	H	68	h	h
49	I	I	69	i	i
4A	J	J	6A	j	j
4B	K	K	6B	k	k
4C	L	L	6C	l	l
4D	M	M	6D	m	m
4E	N	N	6E	n	n
4F	O	O	6F	o	o
50	P	P	70	p	p
51	Q	Q	71	q	q
52	R	R	72	r	r
53	S	S	73	s	s
54	T	T	74	t	t
55	U	U	75	u	u
56	V	V	76	v	v
57	W	W	77	w	w
58	X	X	78	x	x
59	Y	Y	79	y	y
5A	Z	Z	7A	z	z
5B	[	[	7B	{	{
5C	\	\	7C	|	÷
5D	]	]	7D	}	}
5E	↑	↑	7E	~	~
5F	←	_	7F	DEL	▒

Some points to note on the tables above and the previous page:

The characters for 00 and 20 both display as a blank space; 00 can be used as a "graphics" space, and 20 can be used as an "alphanumerics" space. The character for code 5F (ASCII back arrow) displays as the underline character "_". The character for code 60 (ASCII `) displays as "£", code 7C (|) displays as "÷", and code 7F (DEL) displays as a chequerboard pattern (alternating black and white dots). These changes are to comply with convention in some cases, and special requests in others.

Note that if the reverse video option is selected there are a further 128 characters which are simply the reverse video versions of those listed. Their code is found by adding Hex. 80 to the codes listed, so for example 2A is the "*" character, AA (=80+2A) is the same in reverse video.

4.2 Appendix 2: Character Generator EPROM

Section 4.1 of this Manual has given an example of one set of characters for what might be termed a standard character set, which is likely to be adopted by most users of the VDU-K. (A programmed EPROM can be obtained at modest cost by VDDU-K purchasers from the supplier of the VDU-K card.)

However, many users may wish to make minor detail changes to the characters, or of course may wish to devise their own, this being one of the main attractions of the card. (It is often a great benefit to be able to have a preprogrammed set of special characters, since this saves the software overhead suffered by ostensibly more sophisticated systems which have a RAM based set, and thus have to burden the main program with the task of storing the required character set within itself.)

The arrangement of the various data within the character generator EPROM has not been decided lightly. As each bit set to a "1" in the EPROM corresponds to a lighted dot in the finished character (displayed in normal, not reversed, video), it might not be thought important which particular addresses are used, as long as they are defined. The arrangement which has been adopted in the VDU-K design has been carefully chosen to make the design and programming of a custom set of "applications" characters as easy as possible.

For example the first byte of the data to compose the character "A" (ASCII code 41H, the "H" suffix meaning hexadecimal notation) is to be found at the EPROM address 410H, i.e. 41H x 10H, similarly the data for code 62H (ASCII letter "b"), are found at addresses beginning 620H.

As each character cell is eight dots wide, an eight bit byte is ideally suited to the purpose of storing the pattern of dots. The convention used in this design is that the most significant bit is the one which appears at the left-hand side of the character cell, and the least significant bit is the one on the right. This makes it quite easy to visualise characters, since if the byte is written out in binary format the 1's will represent lit dots, and the 0's will represent blank dots. It is perhaps even easier to imagine the appearance of the displayed character if say "*" is used for a "1", and "-" for a "0".

For example if the contents of 410H in the EPROM were 0FH (actually in the standard character generator they aren't, but say they were), then the top line of the character coded 41H would appear as:

```
----****  (since 0FH = 00001111)
```

if they were F0H the top line would be

```
****----  (since F0H = 11110000)
```

(Appendix 2 continued)

Similarly for the following data:

Address (Hex.)	Data	Display	Binary
410	00	--------	00000000
411	10	---*----	00010000
412	28	--*-*---	00101000
413	44	-*---*--	01000100
414	44	-*---*--	01000100
415	7C	-*****--	01111100
416	44	-*---*--	01000100
417	44	-*---*--	01000100
418	00	--------	00000000
419	00	--------	00000000

The example above this time is the actual sequence of ten consecutive bytes which are found in the standard character generator EPROM starting at address 410H, and it may be seen that it represents the letter "A", ASCII code 41H.

Ten consecutive bytes are used to make up the character cell, which is a 8 x 10 matrix of dots. The alphanumeric characters do not extend to the sides of the cell in all directions, as for good legibility a blank space is required between adjacent characters, horizontally, and vertically.

The convention which has been followed in the standard character generator EPROM is to compose all the upper-case (capital) letters on a 5 x 7 matrix, located within the 8 x 10 cell as shown in the example above. For each of the alphanumeric characters the top row of dots in the cell is blank, as is the left column and the two right columns. The lower-case letters are mostly composed on a 5 x 5 matrix which begins two rows lower than the tops of the upper-case letters. Some of the lower-case letters e.g. g, j, p, etc. have "decenders", i.e. the character has parts which are lower than the bottom row of the upper-case letters. Lower-case letters with decenders are composed on a 5 x 7 matrix like the upper-case letters, but displaced downwards by two rows.

(Appendix 2 is continued overleaf.)

(Appendix 2 continued)

If it is required that adjacent characters "join up" then no blank rows or columns should be left. An example of one such character in the standard character generator EPROM is given below; it is the "pixel" character 09H, which is located in the EPROM at address 090H:

Address (Hex.)	Data	Display	Binary
090	F0	****----	11110000
091	F0	****----	11110000
092	F0	****----	11110000
093	F0	****----	11110000
094	F0	****----	11110000
095	0F	----****	00001111
096	0F	----****	00001111
097	0F	----****	00001111
098	0F	----****	00001111
099	0F	----****	00001111

It should be noted that the size of the character cell displayed on the standard VDU-K card is very close to being square. This is of arguable benefit in the case of alphanumeric characters, but it makes the design of graphic displays particularly easy.

The amount of space in the EPROM devoted to each character is, as discussed above, ten consecutive bytes. There are in fact sixteen successive bytes available in the EPROM for each character but the last six are not displayed. They can be any code, for example "FFH", the natural state of an unprogrammed EPROM, or "00H", the code for blank dots, or indeed anything, as these end groups of six bytes are not displayed.

For certain special applications of the VDU-K, some users may substitute a binary counter type 74LS293 for U10 in place of the normal decade counter type 74LS290, since these two devices are pin compatible. If this is done the screen display can no longer be 24 rows of characters, about 16 rows will be the usable maximum, this being a consequence of the fact that each character cell will be increased to display a 8 x 16 matrix of dots. In this case sixteen successive locations in the character generator EPROM will be used for each character instead of the previous 10, plus 6 spare.

Procedure for the Design of Custom "Applications" Characters.

If the application involves a repeating set, such as say a set of chess men then the design of each individual character should be carried out on graph paper. A chess men EPROM has already been designed, and it proved very convenient to make each piece occupy a matrix of 16 x 20 dots, i.e. four character cells, two horizontally, two vertically. Other applications may be best satisfied by a different arrangement of character cells, e.g. representations of say sheep, pigs, and cows (for say kindergarden use, teaching children to read, or perhaps for some serious use down on the farm), could be made

(Appendix 2 continued)

in a matrix of say 32 x 20, i.e. eight character cells each, four horizontally, two vertically.

Once the shape and format has been designed the various dots can be divided into their eight bit bytes, and programmed into the Applications EPROM at convenient locations.

An alternative type of screen display is one which is not repetitive. An example of this would be a representation of a section of the British Isles for say Meteorological use in preparing a weather map. In such an application there would be fixed features, and repetitive ones (e.g. sun and cloud symbols).

At first sight there might be thought to be insufficient character cells available, since at least one is needed for each section of coastline. This latter statement is true, but there will still be plenty of characters left over when it is realised that the British Isles is mostly land, surrounded by mostly sea. Although the sea for example might take the greatest area on the screen it could possibly be represented by just a single "sea" character (ASCII code "43" perhaps, ho ho), leaving plenty for the other details.

As before graph paper should be used to design the screen layout, but before the EPROM is programmed it should be decided what character codes will be used in the area of interest. For totally patternless areas such as geographical displays, it might be most convenient just to fill that area of screen with ascending character codes, e.g. 80H, 81H, 82H, 83H, etc., and program the features required into the appropriate codes, using perhaps a co-ordinate system. Once written the character codes in the video RAM would not change, unless it was desired to replace for example a piece of Wales with a piece of Scotland.

4.3 Appendix 3: Timing Generator EPROM

The TV sync. pulses and other timing pulses are produced by the on-board Z80A-CPU, running a program which is one of those contained in the timing generator EPROM U2. The programs are very simple in concept, but quite complicated in execution.

In this Section of the Manual only an indication of the methods used will be given, for two purposes:

Firstly so that the interested user can say with confidence that he knows the precise purpose of every component part of his Interak 1 System, and secondly to give a certain amount of guidance to those users who are wishing to use the technique to construct their own timing EPROM for some special modification to the VDU-K card, or perhaps even some similar design of their own.

The Z80A-CPU and the EPROM together make one of the very smallest computer systems imaginable. No external RAM is used as the CPU chip itself contains sufficient for the purpose. The principle of operation is very simple and consists of writing chosen data to a storage latch. The outputs of the latch are the required timing signals. In essence, if a "1" is written to a "bit" of the latch its output goes high, and stays high until a "0" is written, at which point it goes low. Since the clock input to the CPU is crystal controlled, the signals obtained from the outputs of the latch are very precisely controlled, and are absolutely stable, and repeatable from VDU-K card to VDU-K card.

The various time intervals required for a TV sync. pulse generator are made up from such short intervals as 2.33 microseconds. (See Section 5.2 of this Manual for the Timing Diagrams). Intractable figures such as this become fairly easy to work with when a 3.0 MHz clock is used for the CPU: With a 3.0 MHz clock 2.33 microseconds is 7 "T" states (a "T" state being the smallest unit of time considered in the operating cycle of a Z80A microprocessor and is the lencth of time for one cycle of the clock). Reference to the precise time of the instructions available in the Z80A's repertoire shows that many of them (e.g. LD (HL),A) are exactly 7 "T" states long. The length of a whole TV line (64 microseconds) is a whole number of "T" states (actually 192), and similarly the time duration for the visible part of the display (42.66 microseconds) is exactly 128 "T" states long.

It should be stressed that when time delays as little as 7 "T" states are required such circuits as a Z80A-CTC (Counter Timer Circuit) provide no benefit. Even with the Z80A-CPU's fast interrupt response the time taken would be much too long, to say nothing of the fact that the extra chips required would remove the outstanding benefit of low cost and small chip count. It is for similar reasons that some of the counting which could have been done in software has in fact been carried out by hardware (e.g. the cost of two four bit counters in the shape of a 74LS393 is not so very different to that of an eight bit latch, especially when extra decoding is added to enable the latch, and as a bonus the hardware counter occupies less board space).

In this design the only thing which is read by the CPU is the EPROM, and the only thing which is written to is the latch, and so there is no need for any decoding or differentiation between I/O space and Memory space; the $\overline{RD}$ (read) line from the CPU enables the EPROM directly, and the $\overline{WR}$ (write) line clocks the latch.

Although the VDU-K card requires only four timing lines (shown on the diagram as V, H, R, S), a six bit latch has been provided to allow for unspecified future applications (for example to provide separate line and frame sync. pulses for TV monitors which cannot accept both line and frame sync. combined).

A novice might be concerned that the action of changing the output of one of the timing lines might disturb one of the others, since all bits in the latch are written to at the same time. There is no need to worry about this as there is in fact no problem. The secret is to remember that if a line is to remain unchanged at a particular point in the timing cycle, it is perfectly acceptable to write data to the appropriate "bits" of the latch, provided they include the same data for those "bits", i.e. continuously writing "1's" on top of "1's" will result in constant unchanging "1's" as outputs, and similarly for "0's" written repeatedly on top of "0's".

In the case of a non-interlaced display each consecutive TV frame has 312 picture lines, and the control program continuously loops round a sequence of instructions which take 312 x 64 microseconds to complete, i.e. 59,904 "T" states, no more, no less. An interlaced display has a sequence which is exactly 625 lines long (ideally suited to a 625-line TV set), i.e. exactly 120,000 "T" states. This latter sequence is divided into two consecutive TV frames, one having 312 picture lines, and the next having 313 (312 + 313 = 625). In the case of an interlaced display the commencement of the frame sync pulse alternates between starting at the beginning of a TV line, and half way through it. The effect of this on the TV screen is to cause adjacent frames of an interlaced display to have lines which are displaced by half the distance between them. This gives a superior display for TV broadcast pictures viewed from a distance of several metres, but the technique is of dubious benefit when computer pictures are viewed close-up. So that all schools of thought may be accommodated, the standard timing generator EPROM supplied includes programs for each format.

There are some diagrams in Section 5.2 of this Manual which illustrate the description in the previous paragraph, but as the authors of the Manual prefer to think of themselves as computer boffins rather than TV boffins, the reader is referred to any book on the principles of television for a fuller and more lucid description.

It is hoped that a full listing of the program will be made available for an appropriate fee, in order to aid any users who wish to write their own, or modify that provided. Such a listing does not exist at the time of writing, since much of the required timing was derived empirically. Part of the reasons for this will be appreciated if the following caution is understood:

Any users who are writing their own timing program should not fall

into the trap of thinking that a given output will persist for the duration of the instruction which caused it. For example it might be thought that an instruction 7 "T" states in long which writes a "1" to the output latch (assumed to be previously "0"), followed by an instruction 10 "T" states long which writes a "0", would result in a positive pulse of duration 7 "T" states. This is not normally the case; in the example above the pulse would have a duration nearer the 10 "T" state mark. The reason for this is that the effect of a write instruction only occurs towards the end of that instruction, the early part being taken up with the op-code fetch, the refresh cycle, and so on. In other words, for the majority of the 7 "T" state instruction above the output was "0", and remains "0". It goes to "1", somewhere near the end, and then remains at "1" for most of the 10 "T" state instruction which follows it. After about 10 "T" states the instruction takes effect and the "1" output returns to "0". To summarise, in this example a 7 "T" state instruction to produce a positive pulse results in a pulse which in fact turns out to be 10 "T" states long.

It can be appreciated that the task of writing a program which depends for its operation on precise selection of instructions having the desired number of "T" states, is a task which is made doubly difficult when the timing must be taken not from the instruction under consideration, but from the instruction which follows it.

The diagrams in Section 5.2 illustrate on example of the results of such labour. The program to produce the desired waveforms is at first extremely difficult to understand because it follows none of the normal logical rules of programming; most of the instructions are concerned solely with filling in time (counted out with meticulous accuracy to the individual "T" state). When the time comes for a decision in the program, for example after 240 visible picture lines have been displayed, and it is time to move into the blank bottom margin, then normal relative conditional jumps cannot be employed, since they take a different number of "T" states according to whether or not the condition has been met. In the same way care has to be taken at the point when the whole program loops back to begin again, to ensure that an extra 10 "T" states are not inserted inadvertently into one of the final picture lines when the jump is made. In the case of the very tiny time interval 2.66 microseconds (i.e. 7 "T" states) the time taken by an absolute conditional jump (10 "T" states) is too long. This happens when the five "half-line equalisation pulses" are to be generated, and it proves expedient to produce these five pulses by writing the code out five times in a row rather than to set up a loop counter, which would be the conventional way in a "normal" program.

Even with this necessary wastefulness of memory space the program to do the whole job occupies only about 0.5K, and there is space for four such programs in the standard type 2716 EPROM. Two of the four programs are switch selectable, and are generally the same format, but for interlaced and non-interlaced displays. The other two are link-selectable (by breaking a small piece of track), and could be some other format, for example a 16-line display instead of 24-lines, or perhaps to suit a 525-line 60Hz TV set instead of the usual 625-line 50 Hz type.

4.4 Appendix 4: VDU RAM Memory Map for Interak 1.

There are 32 x 24 = 768 locations on the VDU screen, each of which corresponds to a unique memory location in the memory map of the computer. The actual addresses will of course depend on the settings of the switches S2a-f, which are under the control of the user of the VDU. However, if they are set to suit ZYMON 2 (i.e. S2a-d 'on', with S2e-h "off"), then the address of the top left-hand corner of the VDU will be F000H, and the addresses will follow consecutively until the bottom right-hand corner of the VDU is reached at address F2FFH.

The table which follows gives the start and end addresses for each row of characters which can be displayed on the VDU screen (the addresses are given in hexadecimal notation, the "H" suffix being omitted to make them a little easier to read).

Row	0 ... 32 Columns ...	31
0	F000	F01F
1	F020	F03F
2	F040	F05F
3	F060	F07F
4	F080	F09F
5	F0A0	F0BF
6	F0C0	F0DF
7	F0E0	F0FF
8	F100	F11F
9	F120	F13F
10	F140	F15F
11	F160	F17F
12	F180	F19F
13	F1A0	F1BF
14	F1C0	F1DF
15	F1E0	F1FF
16	F200	F21F
17	F220	F23F
18	F240	F25F
19	F260	F27F
20	F280	F29F
21	F2A0	F2BF
22	F2C0	F2DF
23	F2E0	F2FF

The purpose of providing the above table is to give a guide for users who are designing a screen display, and therefore need to know where each line of characters begins and ends.

4.5 Appendix 5: Interlaced/Non-Interlaced Display.

The difference between an interlaced and non-interlaced display has been mentioned at appropriate places in this Manual, in the general description, the detailed description, switch settings, timing generator EPROM description, and so on. In each section the subject of interlaced and non-interlaced display has been approached from the point of view of the needs of the user at the time he is reading that section of the Manual.

In this Appendix the subject is covered again simply to provide a handy reference point, to save the casual reader from having to wade through the whole Manual to find the information.

Commonly the type of TV receiver for which the VDU-K is designed is described as "625-line". There are not many people who have tried to count the number of lines on a TV picture and have remained sane, but those who have will be able to confirm that not all are displayed; there are a number missing.

The missing lines occur at the end of the picture when the electron beam which forms the picture is returning to the top of the screen. They are blanked in the TV receiver, because they would spoil the display as they spot is travelling upwards much faster than it travelled down. The blanked lines are known as "frame flyback" lines, and they are only visible on badly adjusted TV receivers.

Thus there are less than 625 lines displayed on a 625 line TV receiver. In fact the 625 lines mentioned above are achieved by an illusion, only present in an "interlaced" display. In an interlaced display consecutive "frames" are alternately "odd" and "even". (A "frame" is a complete scan of the whole screen, which takes place in 20 milliseconds, i.e. one fiftieth of a second, as there are fifty frames displayed per second.) Since there are two types of frame, "odd" and "even" it can be seen that there are twenty-five of each type to make up the total of fifty. Including the blank lines, there are 312.5 lines to each frame in an interlaced display. The consecutive odd and even frames are displaced vertically by one half the distance of separation of adjacent lines by an ingenious method of timing the frame synchronisation pulse, and due to the effect known as "persistence of vision" the viewer sees both sets simultaneously (excluding of course the invisible blanked lines) and thus observes 312.5 + 312.5 = 625 lines, Q.E.D.

The ingenious method referred to above was devised by the television engineers of long ago and is to arrange that the frame flyback starts half way along the the last line of an odd field, and at the end of the last line of an even field. Successive fields therefore start at a time which is different to the preceding field to the extent of half a line, which results in a vertical difference of one half the spacing of adjacent scan lines.

At the end of this Section of the Manual there is a diagram which attempts to clarify the above description, and demonstrate visually the difference between an interlaced and a non-interlaced TV display.

(Appendix 5 continued)

It will be seen in the case of the interlaced display that the number of lines displayed for each frame is a whole number, which may seem to conflict with the description above referring to a fractional number (312.5). This is fairly easily resolved when it is appreciated that the time taken for the frame flyback includes the missing half line.

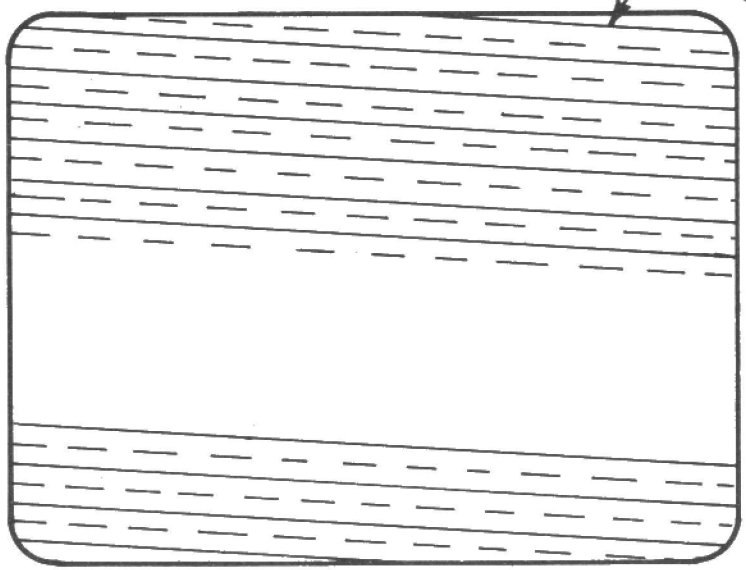
By comparison, the non-interlaced display is quite simple. In a non-interlaced display all fields are the same "hybrid" type i.e. they start as "odd" fields and finish as "even". The extra half line which was used to cause the alternation of frames to give the interlaced display is removed, and each frame consists of 312 lines. Consequently the time taken to complete fifty frames is reduced slightly, and the frame frequency is thus increased from 50.00 Hz to 50.08 Hz. This is entirely insignificant in this application. (It would however be important if the signals from this card were being blended into an existing TV display, e.g. to insert subtitles etc. into a broadcast TV picture. In such a case the 12.0 MHz master crystal would have to be reduced in frequency slightly, or perhaps more practically, the interlaced option of the timing generator should be chosen for this application instead of non-interlaced.)

Ostensibly the interlaced format is the superior one, and indeed it is for moving conventional broadcast TV pictures. Viewed from a few metres away the scan lines can hardly be seen. However things are a little different for close-up viewing of computer style material. Many people report a disturbing flicker which makes the interlaced display less than ideal for viewing for a long time. The probable reason is that each of the two types of frame ("odd" and "even") in an interlaced display is only repeated every other frame, i.e. twenty five times per second. This frequency is low enough to cause visible flicker, particularly when, as is the case in a typical computer display, there are only sharp changes from white to black, rather than hazy changes of intensity from white via grey to black.

When this point is considered it can be seen that there is a chance that a non-interlaced display may prove to be without the disadvantages mentioned above. As the same frame is repeated fifty times a second rather than the twenty five times a second, which is the case when the "even" frame is interlaced with the "odd" one, the resulting picture is much steadier, and in most cases is preferred by users who spend a lot of time close up to their screen.

If special computer display monitors with long-persistence phosphors are used then the effect of flicker is much less pronounced and the interlaced display might give subjectively superior results. (Note that although long persistence phosphors are often green, the reverse is not true. Green screens on TV monitors are most often not long-persistence types. This could have a lot to do with the description "TV monitor"; if a monitor is actually to be used for TV pictures, it cannot really have a long persistence screen, because if it did it would give a most unacceptable "smearing" of quick movement in pictures on the screen.)

INTERLACED DISPLAY

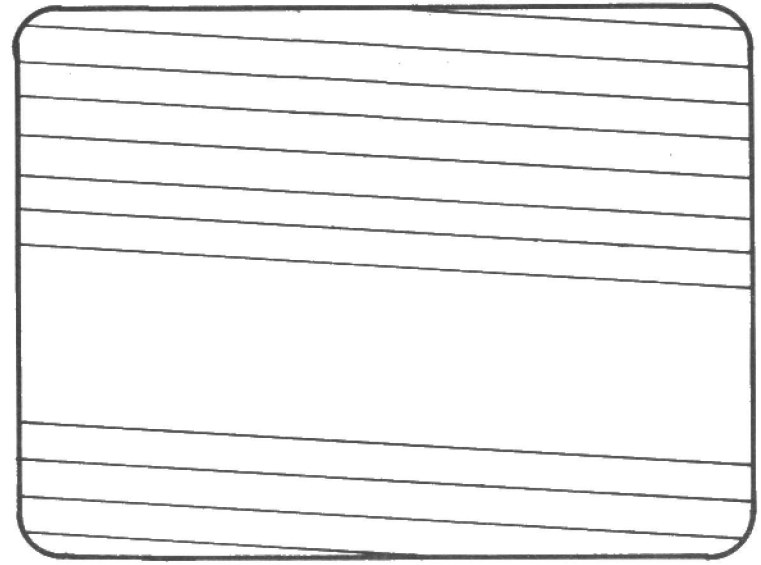


——— ODD FIELD — — — EVEN FIELD

THE 312½ LINES IN THE ODD FIELD ARE 'INTERLACED' WITH THE 312½ LINES IN THE EVEN FIELD TO FORM THE CONVENTIONAL 625-LINE TV DISPLAY (312½ + 312½ = 625). NOT ALL THE LINES ARE VISIBLE, AND THE '½' LINE IN EACH FRAME IS ABSORBED DURING THE FRAME FLYBACK TIME, WHICH IS NOT A WHOLE NUMBER OF LINES.

NOTE THAT THE INDIVIDUAL PICTURE ELEMENTS ARE REFRESHED ONLY IN ALTERNATE FRAMES, HENCE A LONG-PERSISTENCE PHOSPHOR IS NEEDED TO AVOID FLICKER WHEN THE SCREEN IS VIEWED CLOSE UP. (HOWEVER A LONG PERSISTENCE PHOSPHOR WILL CAUSE 'SMEARING' IF THE PICTURE INCLUDES ANY ANIMATED ELEMENTS, SO SOME TRADE-OFFS ARE INVOLVED IN INTERLACED DISPLAYS.

NON-INTERLACED DISPLAY



A 'HYBRID' FIELD (STARTS 'ODD', FINISHES 'EVEN'), IS REPEATED IN EVERY CONSECUTIVE FRAME. INDIVIDUAL PICTURE ELEMENTS ARE THEREFORE REFRESHED IN EVERY FRAME, I.E. TWICE AS OFTEN AS IN THE INTERLACED DISPLAY. IN MANY CASES A STEADIER, MORE PLEASING PICTURE IS THE RESULT, PARTICULARLY ON A SCREEN WITH A SHORT-PERSISTENCE PHOSPHOR (E.G. A VIDEO MONITOR, WITH OR WITHOUT GREEN SCREEN, OR A DOMESTIC T.V. RECEIVER).

Drawn	D.M.P
Date	9.11.82
Scale	-

Interak

COMPARISON OF INTERLACED DISPLAY FORMAT WITH NON-INTERLACED FORMAT

1 OF 1

4.6 Appendix 6. Effect of A.C. Coupling in Video Circuits.

At the end of this Section is a diagram which illustrates the effect. It is a symbolic diagram rather than an actual picture of a video waveform, and it shows the effect of a.c. coupling in video circuits. In general, the effect of a.c. coupling is detrimental, and for this reason the video output from the VDU-K card is not connected via a coupling capacitor.

From the diagram it can be seen that the average (sometimes called the "d.c.") level of a video signal which is a.c. coupled will depend quite markedly on the picture content. (This effect is due to a property of a.c. coupled circuits, and any text-book on basic a.c. theory will provide further explanation should the reader require it.) If there is a lot of white in the picture, the average level will sink down, and it will rise again if the picture contains a lot of black instead of white. The TV receiver or monitor will have contrast and brilliance controls which will permit a good picture to obtained for one or other of these extremes but not both. The diagram shows that if a setting is found which is right for one condition it will not be right for the other.

This subject is raised here simply so that the user who finds this trouble will not mislead himself into thinking there is something wrong with his VDU-K card; the "fault" is in the TV or monitor.

The effect will be demonstrated most clearly if the TV or monitor controls are adjusted for a picture which is predominantly black, with just one or two words displayed normally. If a program is then run which turns most of the screen white (e.g. a program which writes a lot of inverse video characters on the screen), then it is often the case that the orignal (normal video) characters will become almost illegible until the brilliance and contrast controls are adjusted on the T.V. monitor. This is due to the shift in average level in the video signal, which is demonstated on the diagram.

It is generally not possible to d.c. couple the video throughout in the TV receiver or monitor because of the difficult circuit design problems this would cause, however a top-quality TV receiver or video monitor will have a few extra components added in its circuit to provide a feature known as "black-level clamp". With this feature the undesirable effect of a.c. coupling the video signal will be removed, as the black level clamp forces the black level (and thus the white level) to be held at a fixed potential, so that it does not change with picture content.

Almost all TV receivers are built on a very low budget and their designers cannot justify the luxury of "black level clamping". Partly the reason is to do with the demands this would place on the regulation of the set's E.H.T. (Extra High Tension, i.e. high voltage) supply. As a.c. coupling in the video circuits results in an all black screen being lightened to grey, and/or an all white screen being darkened, there is far less change than there would otherwise be in the demands made on the E.H.T. supply (which would otherwise be very low for a black screen and very high for a white screen). The very

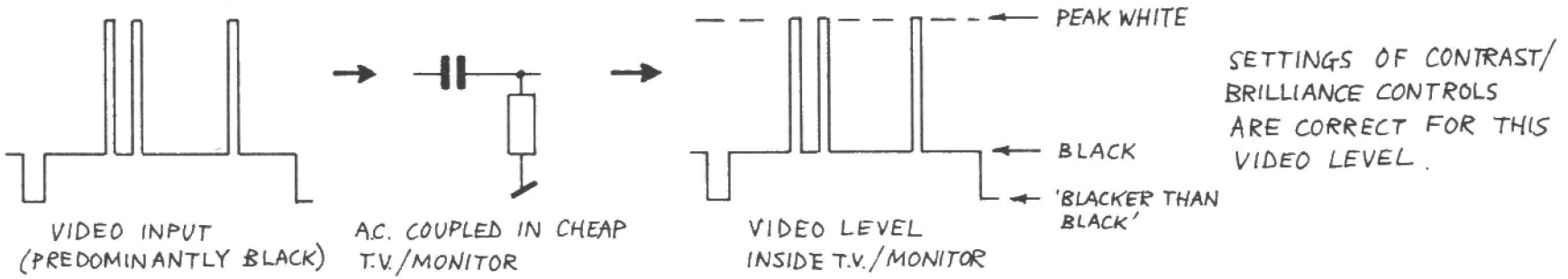
(Appendix 6 continued)

poor E.H.T. regulation on some sets is very visible on those which change the size of the picture according to the intensity of the picture being transmitted.

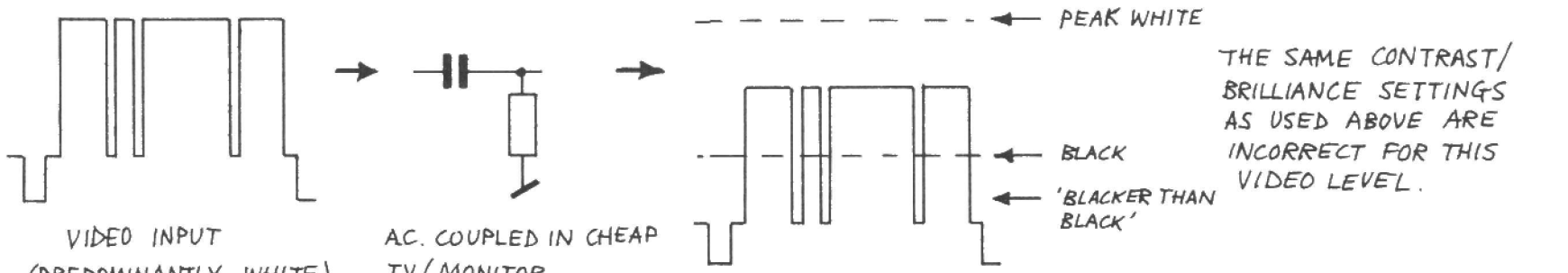
It might be thought that a video monitor would not suffer these defects being built to far more stringent standards (and thus costing a lot more into the bargain!). However nowadays most so-called monitors are nothing more than T.V. receiver designs simply with the aerial and tuning circuitry stripped out and a green phosphor screen fitted, and so they inherit the deficiencies of the T.V. receivers from which they are derived.

There is little that can be done to improve matters if the described effect causes any incovenience; even if the minor circuit changes required to provide "black level clamp" can be devised, they should not be undertaken lightly since they may result in an intolerable burden being placed on the insulation and general construction of the E.H.T. supply if its voltage is caused to rise significantly.

As stated before in this Manual, the authors do not feel highly qualified as teachers when it comes to discussing matters of this kind, and so the reader is directed to seek guidance from a any suitable reference book on the subject of television receiver and T.V. monitor design and kindred matters.



SETTINGS OF CONTRAST/ BRILLIANCE CONTROLS ARE CORRECT FOR THIS VIDEO LEVEL.



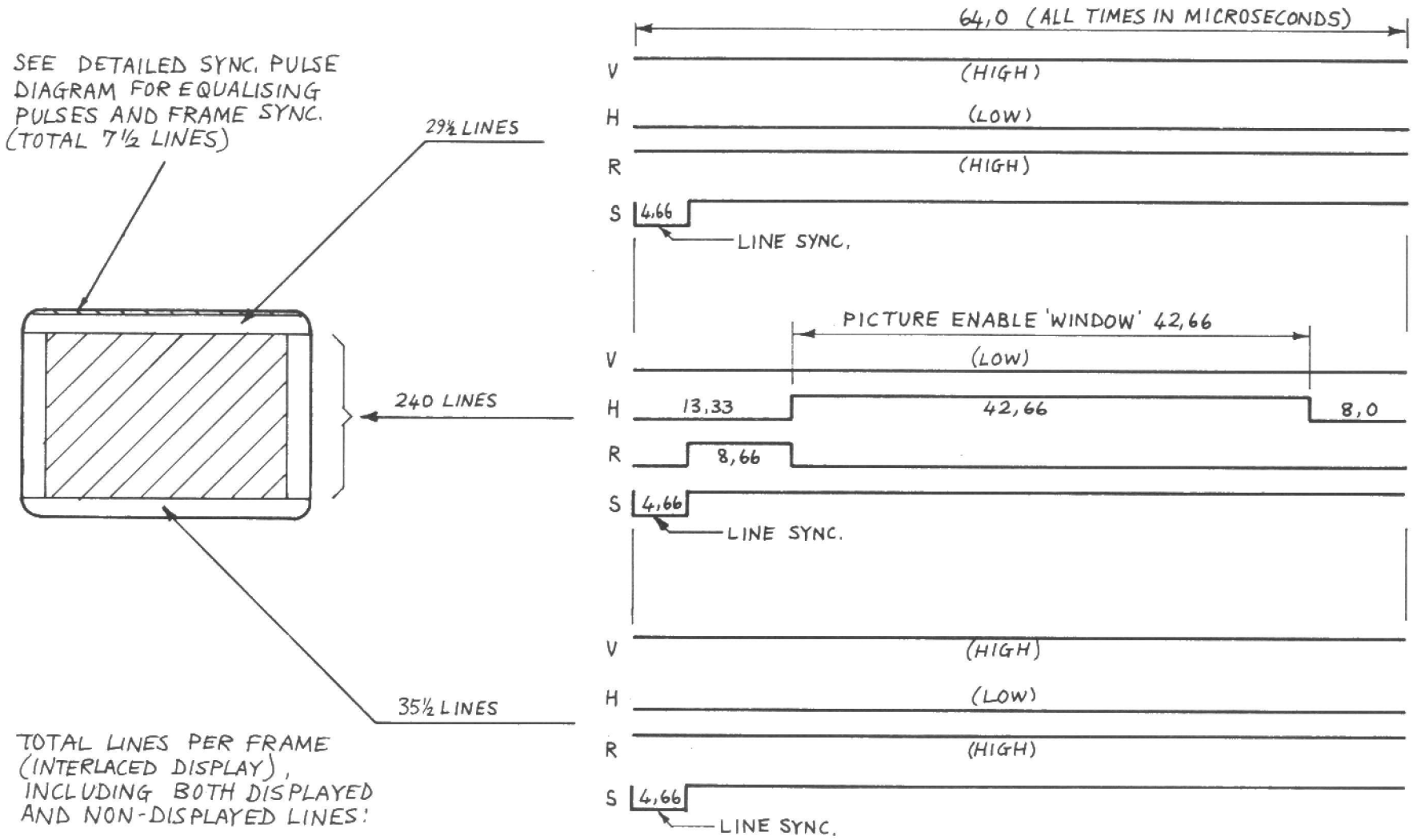
THE SAME CONTRAST/ BRILLIANCE SETTINGS AS USED ABOVE ARE INCORRECT FOR THIS VIDEO LEVEL.

	Drawn D.M.P	Interak
	Date 9.11.82	EFFECT OF A.C. COUPLING IN VIDEO CIRCUITS (D.C. SHIFT WITH PICTURE CONTENT)
	Scale -	1 OF 1

5.1 VDU-K BUS ALLOCATIONS (Note "B" side not used)

1A.	(NIOREQ)	(I/O Request)
2A.	NMREQ	Memory Request
3A.	NWDS	Write Data Strobe
4A.	NRDS	Read Data Strobe
5A.	AB15	Address Bus
6A.	AB14	Address Bus
7A.	AB13	Address Bus
8A.	AB12	Address Bus
9A.	AB11	Address Bus
10A.	AB10	Address Bus
11A.	AB9	Address Bus
12A.	AB8	Address Bus
13A.	AB7	Address Bus
14A.	AB6	Address Bus
15A.	AB5	Address Bus
16A.	AB4	Address Bus
17A.	AB3	Address Bus
18A.	AB2	Address Bus
19A.	AB1	Address Bus
20A.	AB0	Address Bus
21A.	(NRST)	(Reset)
22A.	DB7	Data Bus
23A.	DB6	Data Bus
24A.	DB5	Data Bus
25A.	DB4	Data Bus
26A.	DB3	Data Bus
27A.	DB2	Data Bus
28A.	DB1	Data Bus
29A.	DB0	Data Bus
30A.	(N1IN)	(Daisy Chain)
31A.	(N1OUT)	(Daisy Chain)
32A.	NRFSH	Dynamic RAM Refresh
33A.	(Ø)	(4.0 MHz Z80A Clock)
34A.	(NWAIT)	(Wait State Request)
35A.	(+12V)	(Power Supply)
36A.	(+12V)	(Power Supply)
37A.	Po1	Polarisation Slot
38A.	(-12V)	(Power Supply)
39A.	(-12V)	(Power Supply)
40A.	0V	Power Supply
41A.	0V	Power Supply
42A.	+5V	Power Supply
43A.	+5V	Power Supply

Signals named in brackets are not used by the card; NRFSH on A32 is used but need not be connected in systems which have no signal on this line. In such circumstances the line should be pulled up to a logic "1" (there is space for a pull-up resistor on the VDU-K card if required). The VDU-K card can be used without modification on ISBUS-A (The Interak 1 bus), KBUS-5, and KBUS-12, (the two variants of KBUS).



TOTAL LINES PER FRAME (INTERLACED DISPLAY), INCLUDING BOTH DISPLAYED AND NON-DISPLAYED LINES:

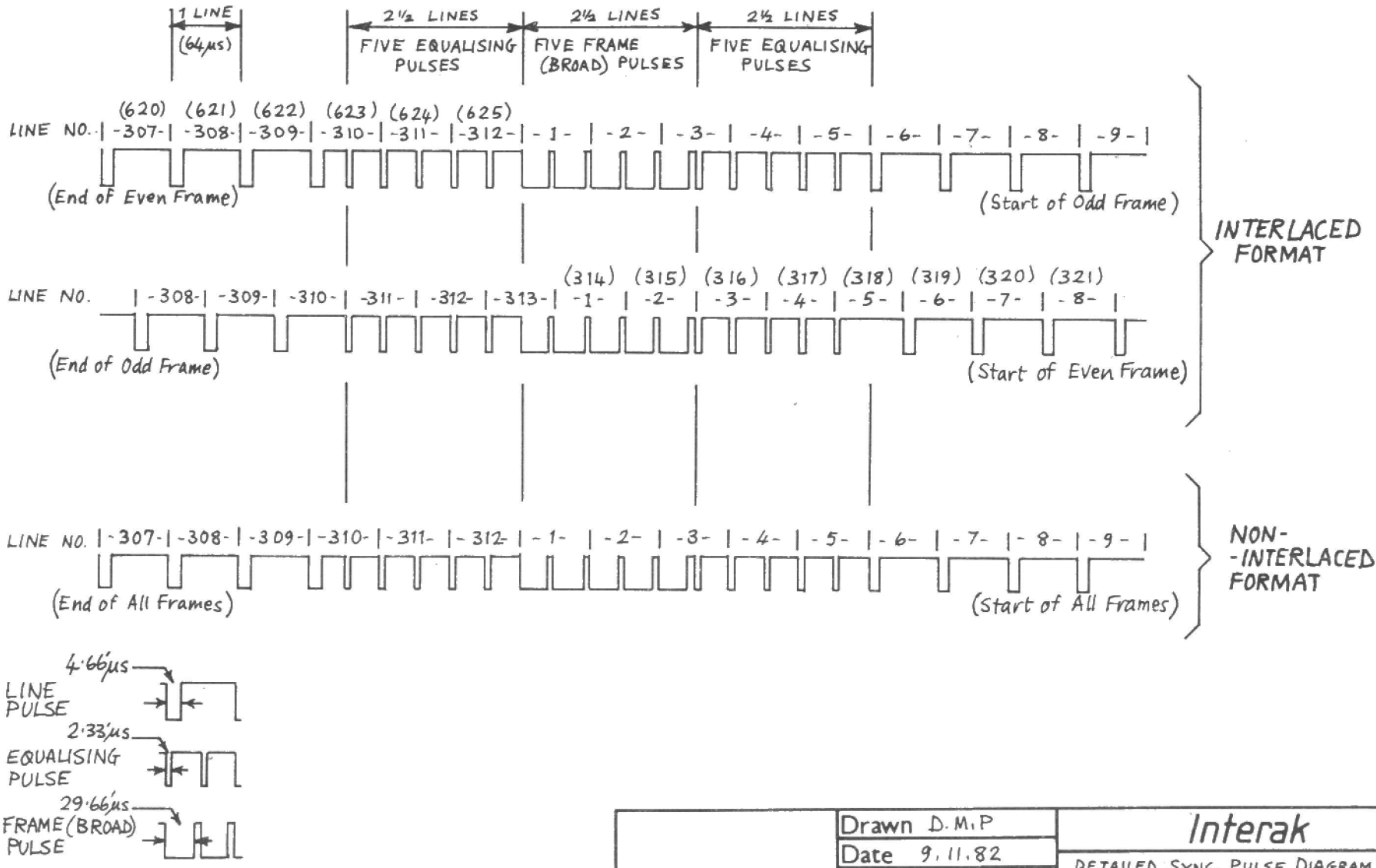
$7\frac{1}{2} + 29\frac{1}{2} + 240 + 35\frac{1}{2} = 312\frac{1}{2}$

Drawn	D.M.P.
Date	9-11-82
Scale	2mm = 1μs

Interak

TIMING DIAGRAM FOR VDU-K USING STANDARD TIMING GENERATOR PROGRAM

1 OF 1

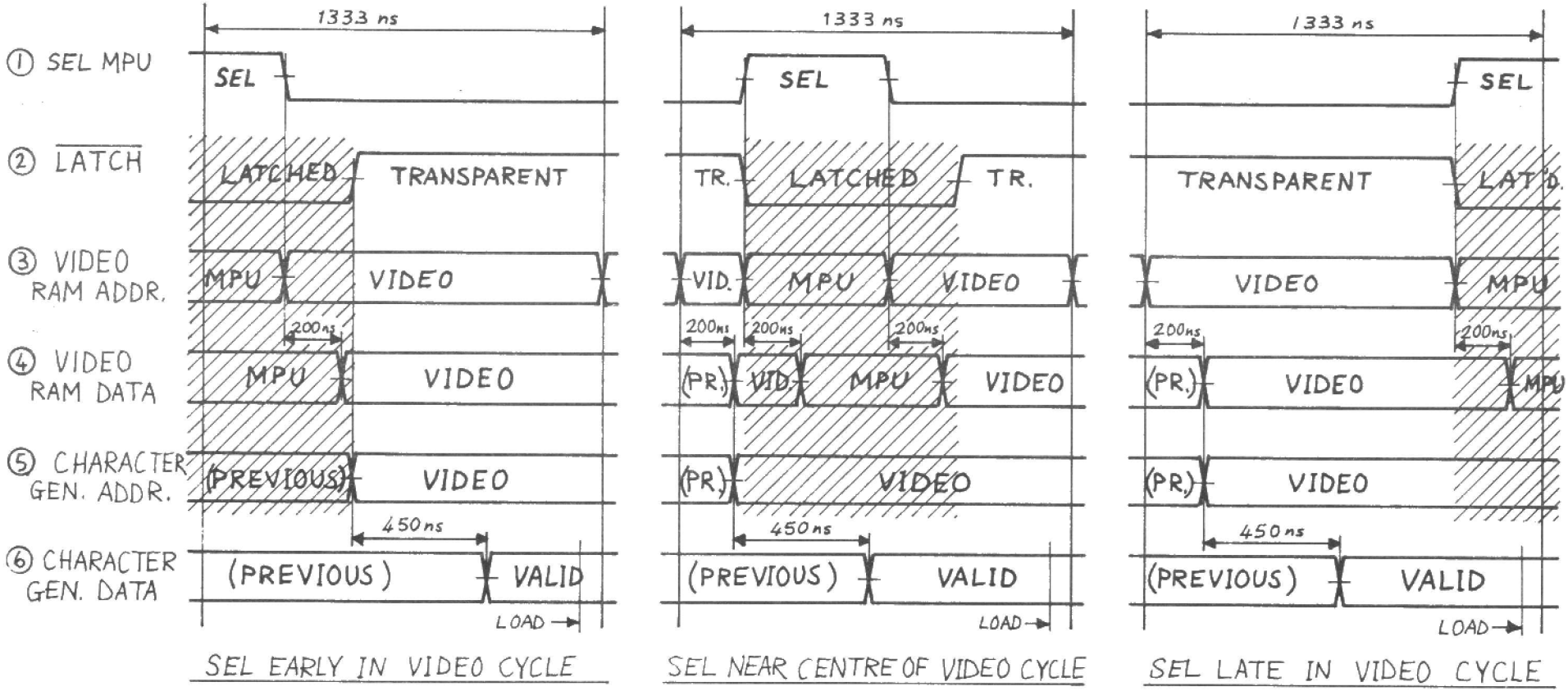


Drawn	D. M. P
Date	9. 11. 82
Scale	12mm = 64μs

Interak

DETAILED SYNC. PULSE DIAGRAM FOR INTERLACED / NON-INTERLACED FORMATS.

1 OF 1

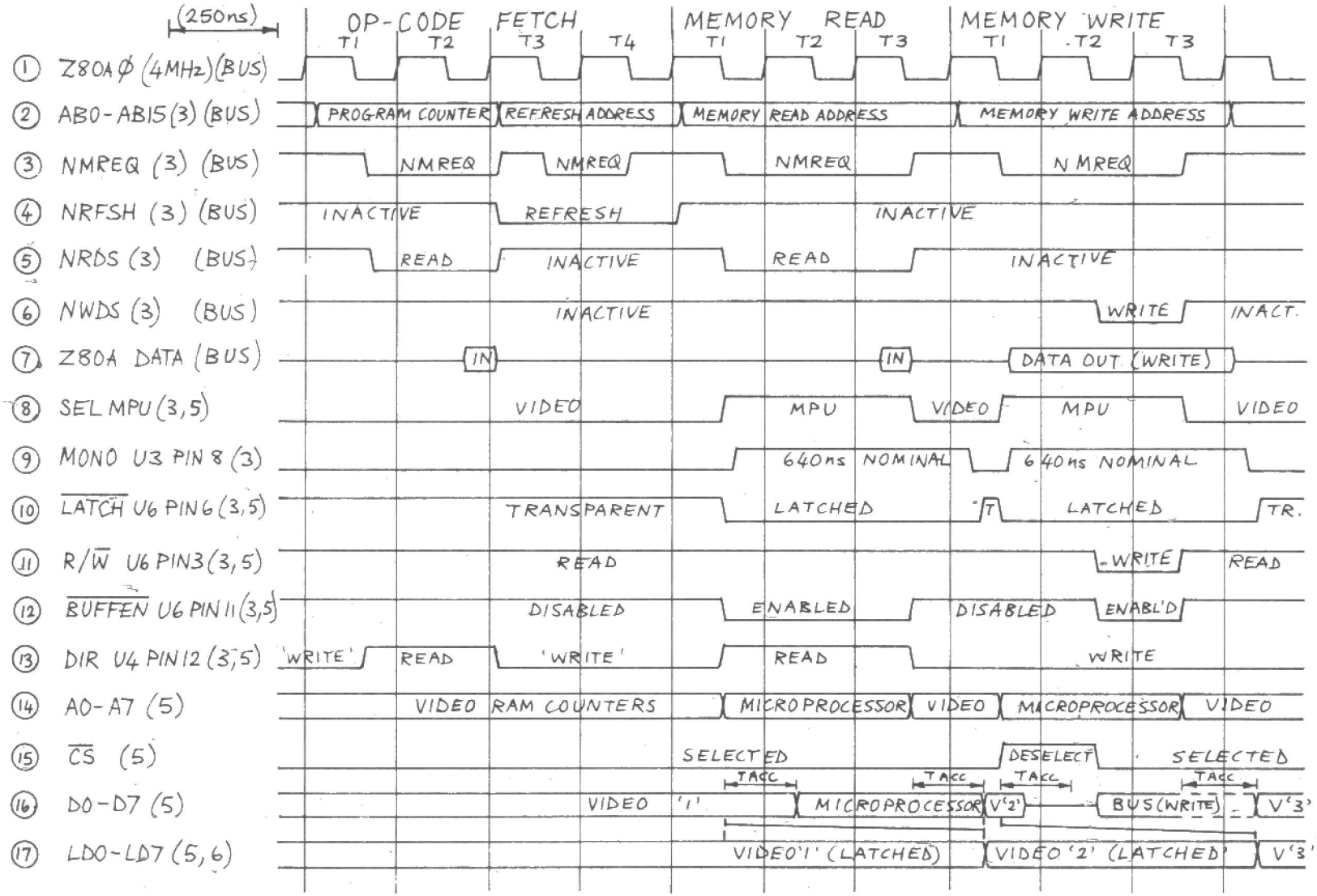


Drawn	D. M. P.
Date	9. 11. 82
Scale	–

Interak

TIMING DIAGRAM FOR MICROPROCESSOR ACCESS, SHOWING 'ANTI-SNOW' FEATURE

1 OF 1



FIGURES IN BRACKETS INDICATE SHEET NOS. OF CIRCUIT DIAGRAM

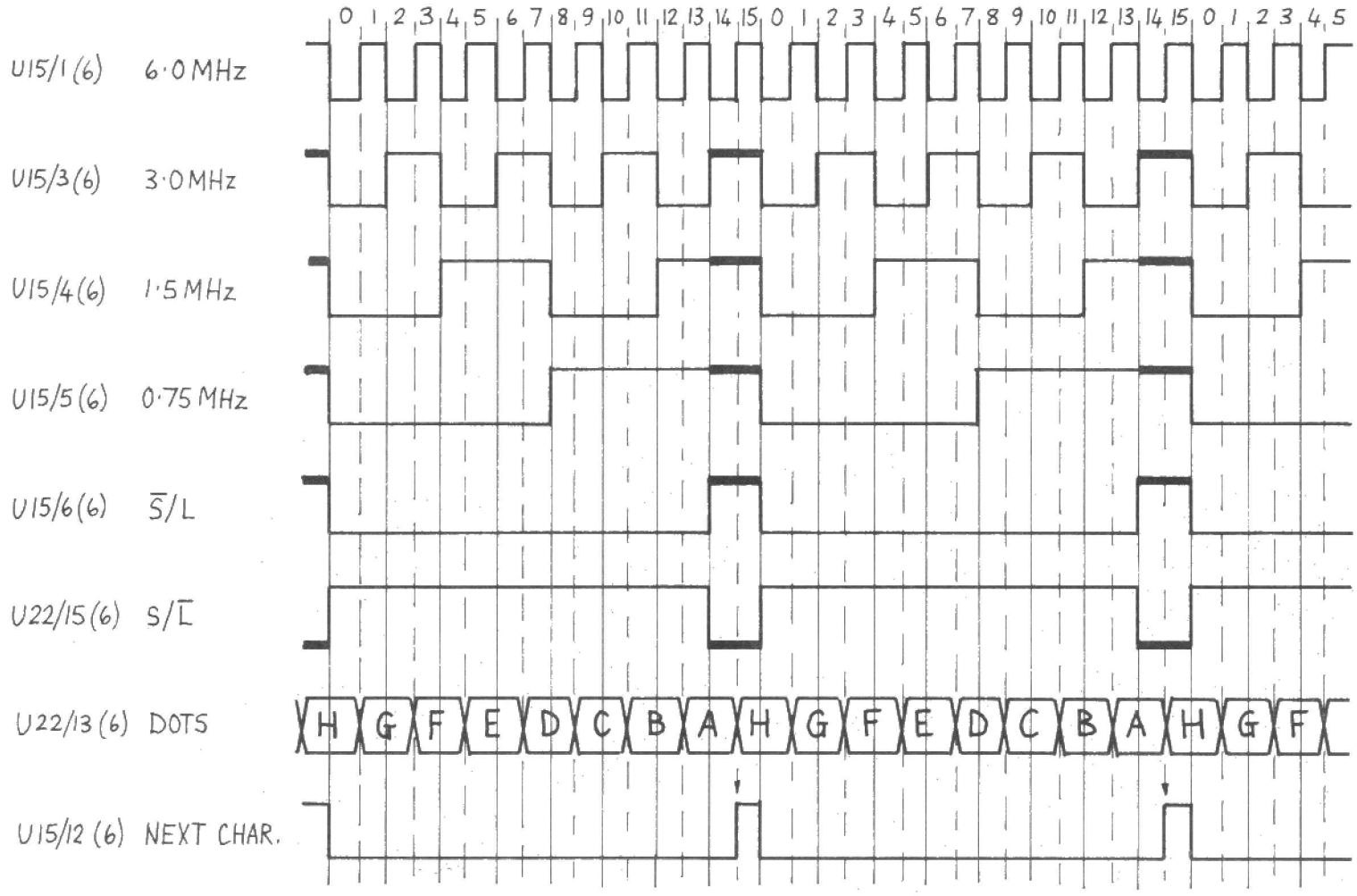
EG. WAVEFORM ⑧ 'SEL MPU (3,5)' MEANS THIS SIGNAL IS TO BE FOUND ON SHEETS 3 & 5.

Drawn	D.M.P.
Date	9.11.82
Scale	-

Interak

TIMING DIAGRAM FOR MICROPROCESSOR ACCESS EXECUTING 'BLOCK MOVE'

1 OF 1



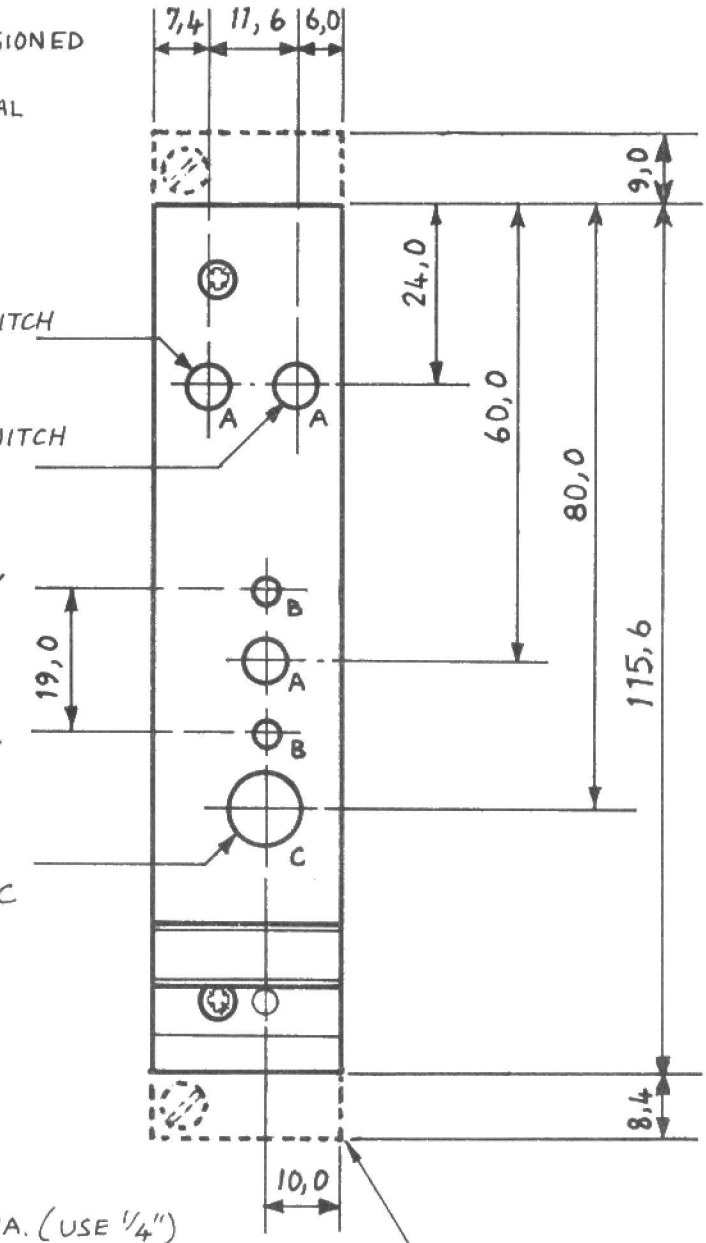
Drawn	D.M.P.
Date	9.11.82
Scale	-

Interak

TIMING DIAGRAM FOR DOT RATE SHIFT REGISTER AND LOADING

1 OF 1

FEATURES NOT DIMENSIONED ARE PRESENT ON THE STANDARD 1 INCH METAL FRONT PANEL.



HOLE FOR OPTIONAL SWITCH S1' (8TH BIT INV/ALT).

HOLE FOR OPTIONAL SWITCH S3 (REVERSE VIDEO).

HOLES FOR T.V. AERIAL CONNECTOR J1.

HOLE FOR OPTIONAL COMPOSITE VIDEO BNC CONNECTOR, J2.

DRILLING DETAILS.

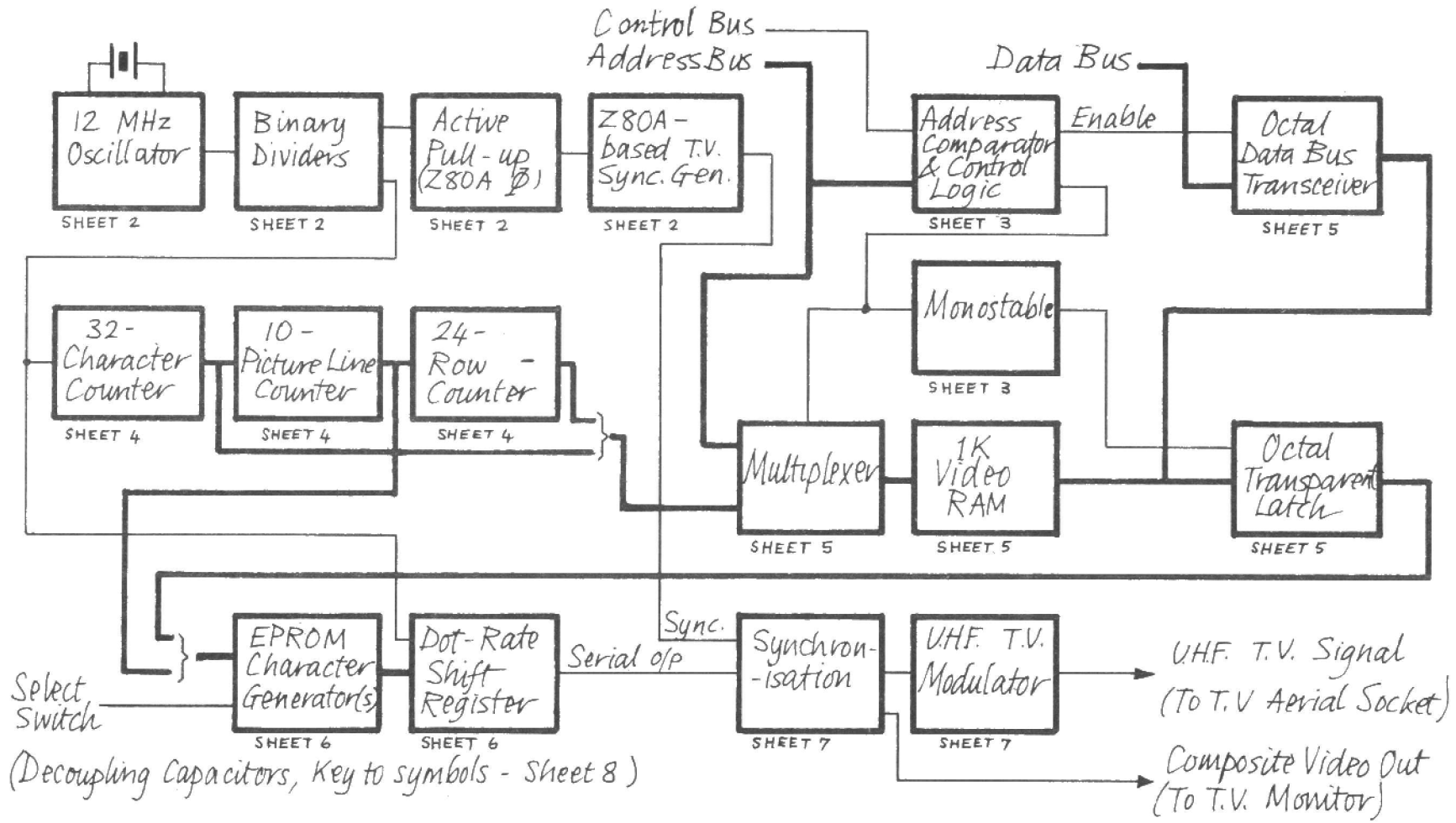
3 'A' HOLES 6,35 DIA. (USE 1/4")

2 'B' HOLES 3,10 DIA. (USE 1/8")

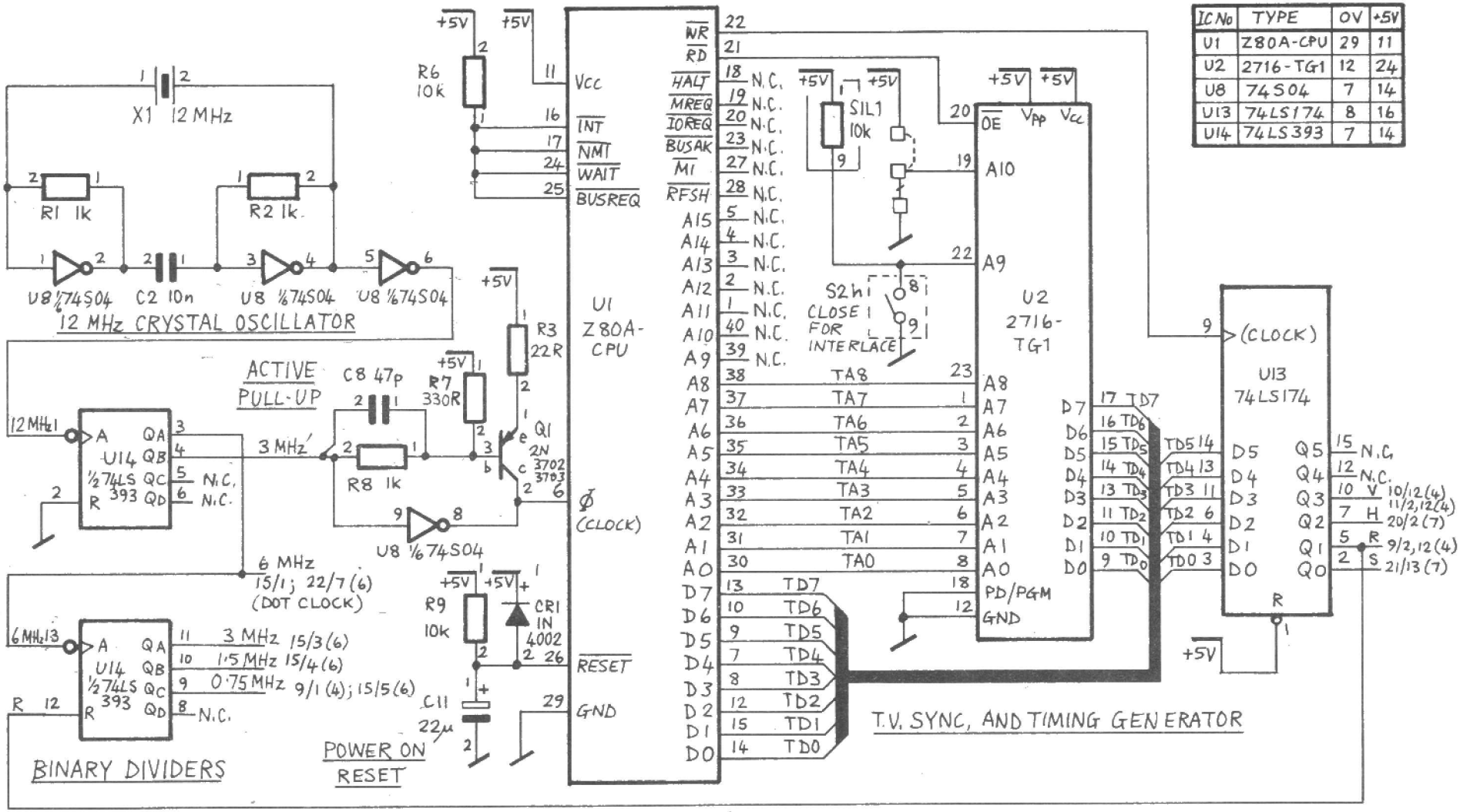
1 'C' HOLE 9,7 DIA. (USE 3/8")

NOTE: THE SOLID CARD FRONT OUTLINE SHOWS THE "NEW TYPE" FRONT PANEL; THE DOTTED EXTENSIONS SHOW THE "OLD (RS) TYPE" FRONT PANEL.

Modified 9.5.83 to show "New Type" Panel Dims.	Drawn D.M.P	Interak
	Date 9-11-82	VDU-K FRONT PANEL DRILLING ETC. DETAILS.
	Scale 1:1	
	Dims. mm	1 OF 1

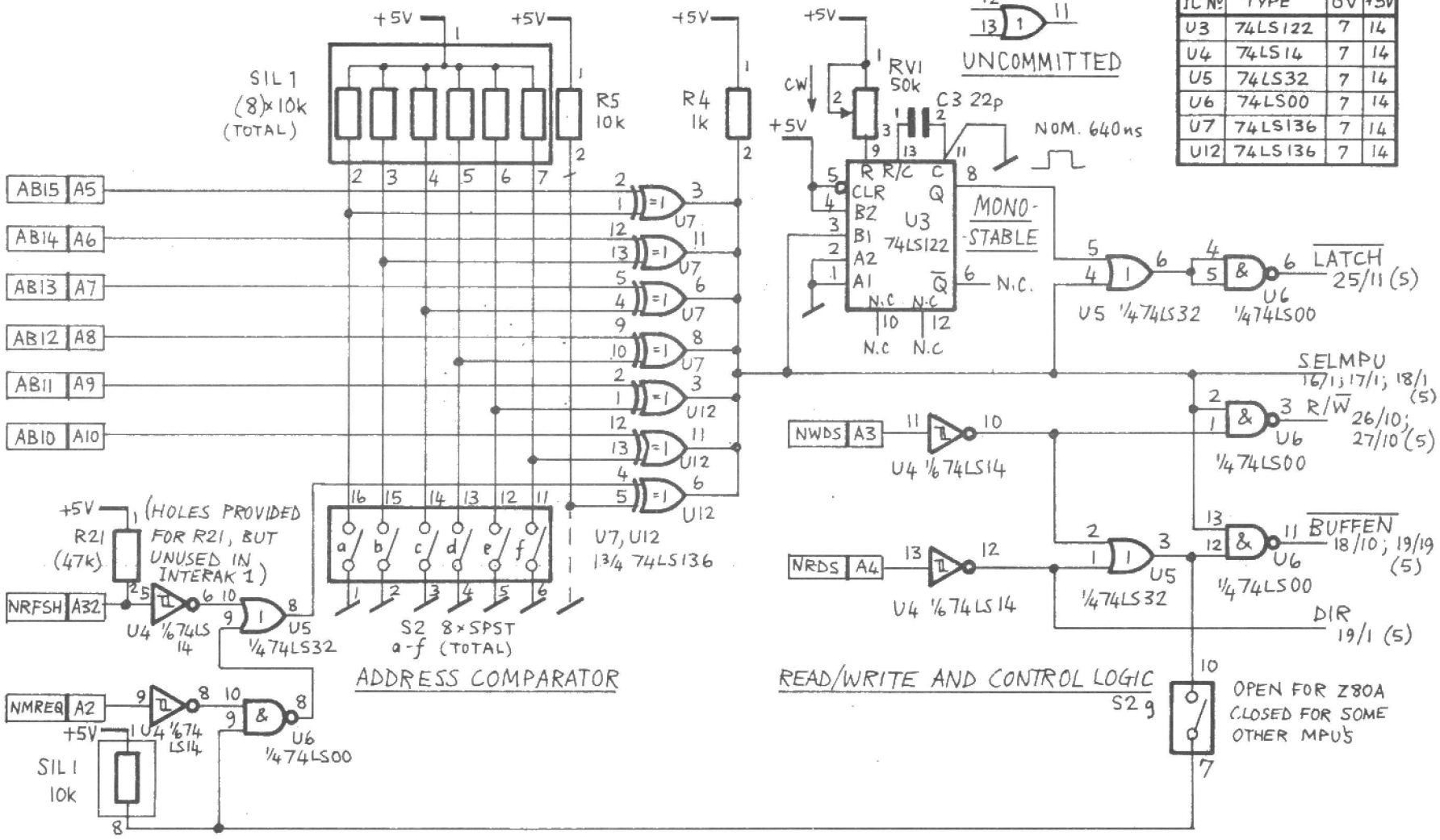


	Drawn D.M.P	Interak
	Date 9.11.82	VDU-K CIRCUIT DIAGRAM, SHEET 1: BLOCK DIAGRAM
	Scale –	1 OF 8



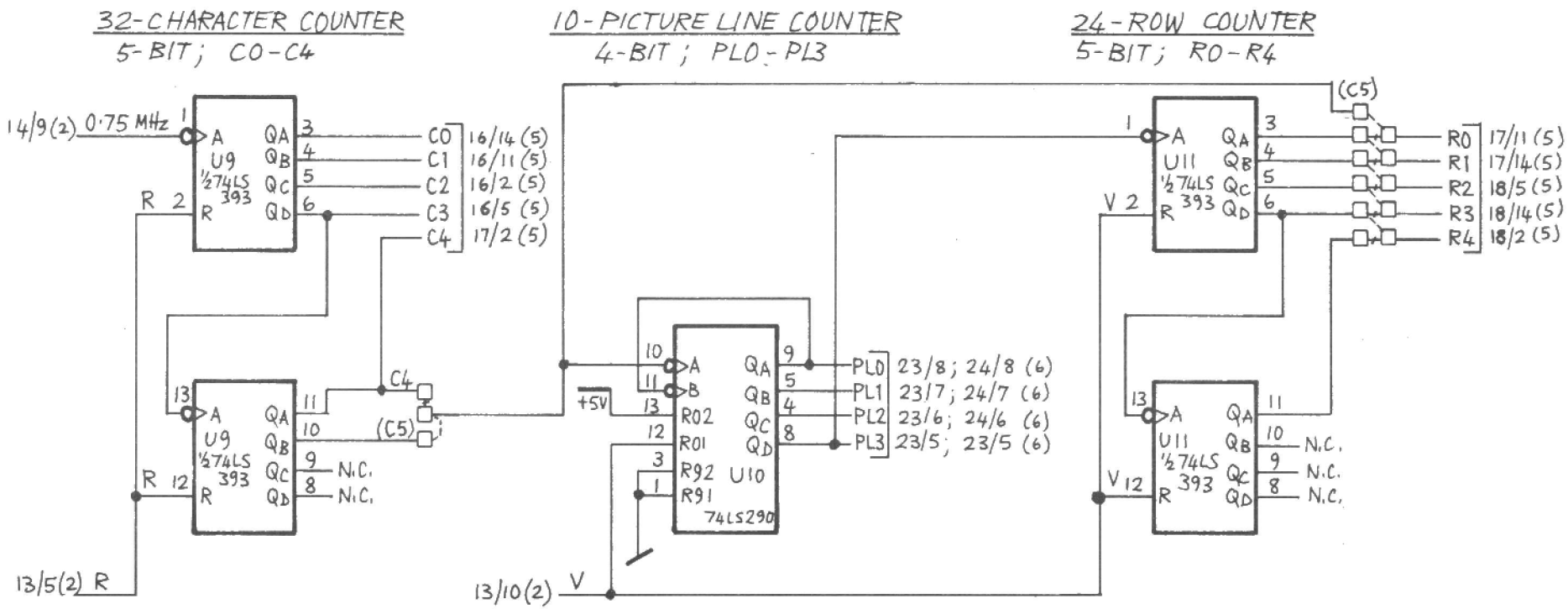
IC No	TYPE	0V	+5V
U1	Z80A-CPU	29	11
U2	2716-TG1	12	24
U8	74S04	7	14
U13	74LS174	8	16
U14	74LS393	7	14

	Drawn D.M.P	Interak
	Date 9.11.82	VDU-K CIRCUIT DIAGRAM, SHEET 2: OSCILLATOR, DIVIDERS, AND SYNC. GENERATOR
	Scale –	2 OF 8



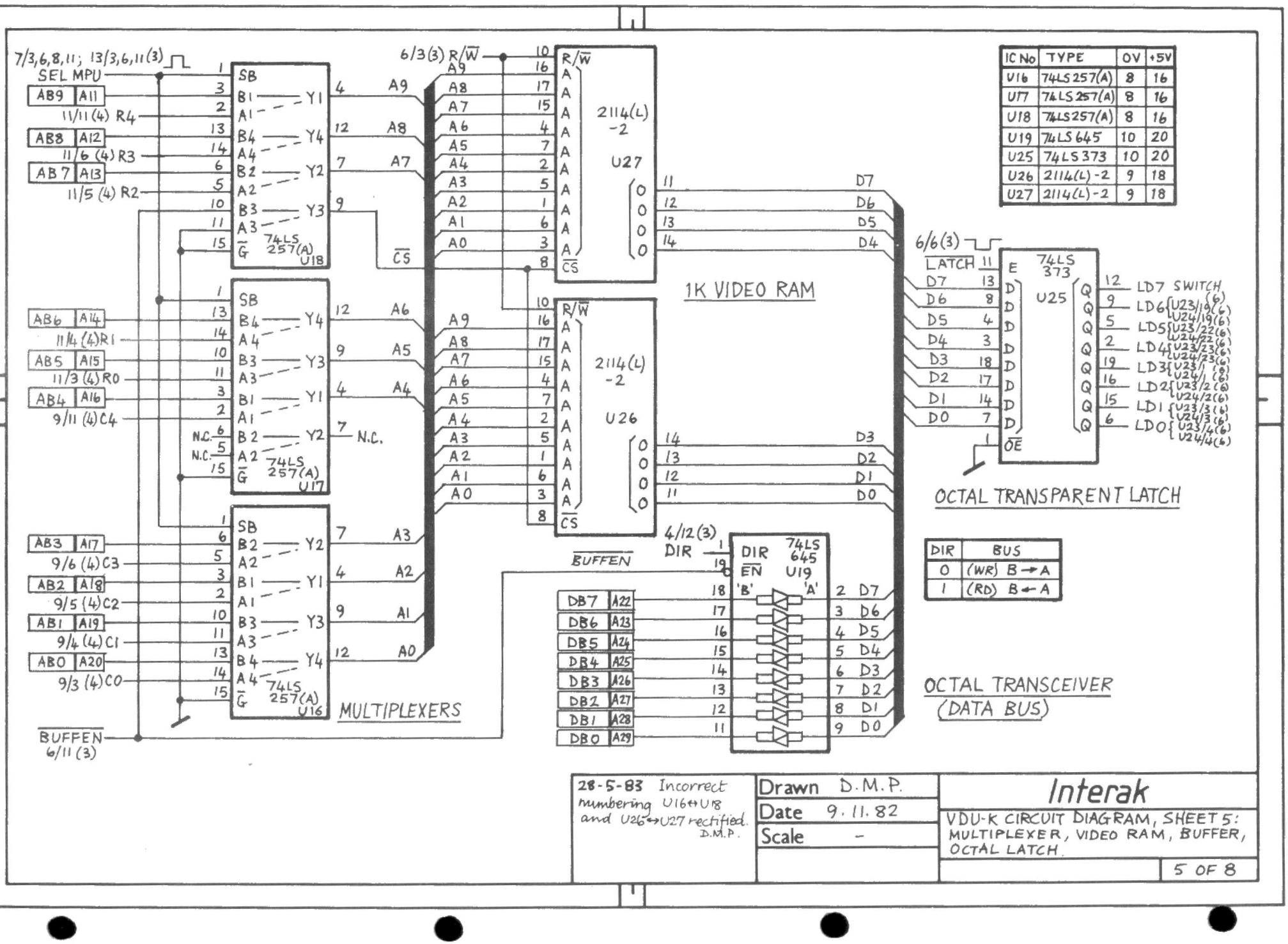
IC Nº	TYPE	0V	+5V
U3	74LS122	7	14
U4	74LS14	7	14
U5	74LS32	7	14
U6	74LS00	7	14
U7	74LS136	7	14
U12	74LS136	7	14

	Drawn D.M.P.	Interak
	Date 9.11.82	VDU-K CIRCUIT DIAGRAM, SHEET 3: ADDRESS COMPARATOR, AND CONTROL LOGIC
	Scale –	3 OF 8



IC No.	TYPE	0V	+5V
U9	74LS 393	7	14
U10	74LS 290	7	14
U11	74LS 393	7	14

	Drawn D.M.P.	Interak
	Date 9.11.82	VDU-K CIRCUIT DIAGRAM, SHEET 4: 32-CHARACTER COUNTER, 10-PICTURE-LINE COUNTER, 24-ROW COUNTER
	Scale –	4 OF 8



IC No	TYPE	0V	+5V
U16	74LS257(A)	8	16
U17	74LS257(A)	8	16
U18	74LS257(A)	8	16
U19	74LS645	10	20
U25	74LS373	10	20
U26	2114(L)-2	9	18
U27	2114(L)-2	9	18

DIR	BUS
0	(WR) B → A
1	(RD) B ← A

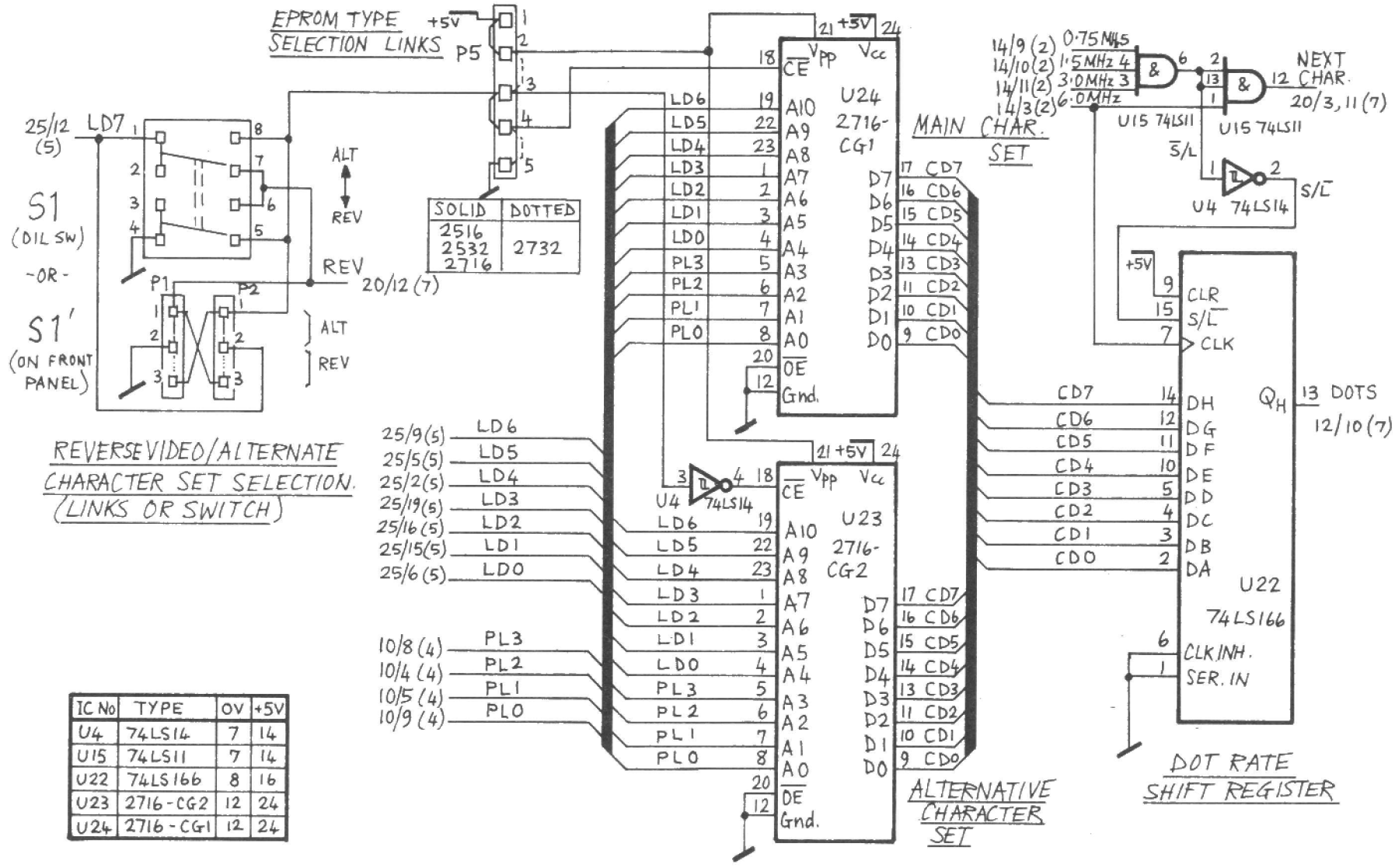
28-5-83 Incorrect numbering U16↔U18 and U26↔U27 rectified. D.M.P.

Drawn D.M.P.
Date 9.11.82
Scale -

Interak

VDU-K CIRCUIT DIAGRAM, SHEET 5: MULTIPLEXER, VIDEO RAM, BUFFER, OCTAL LATCH.

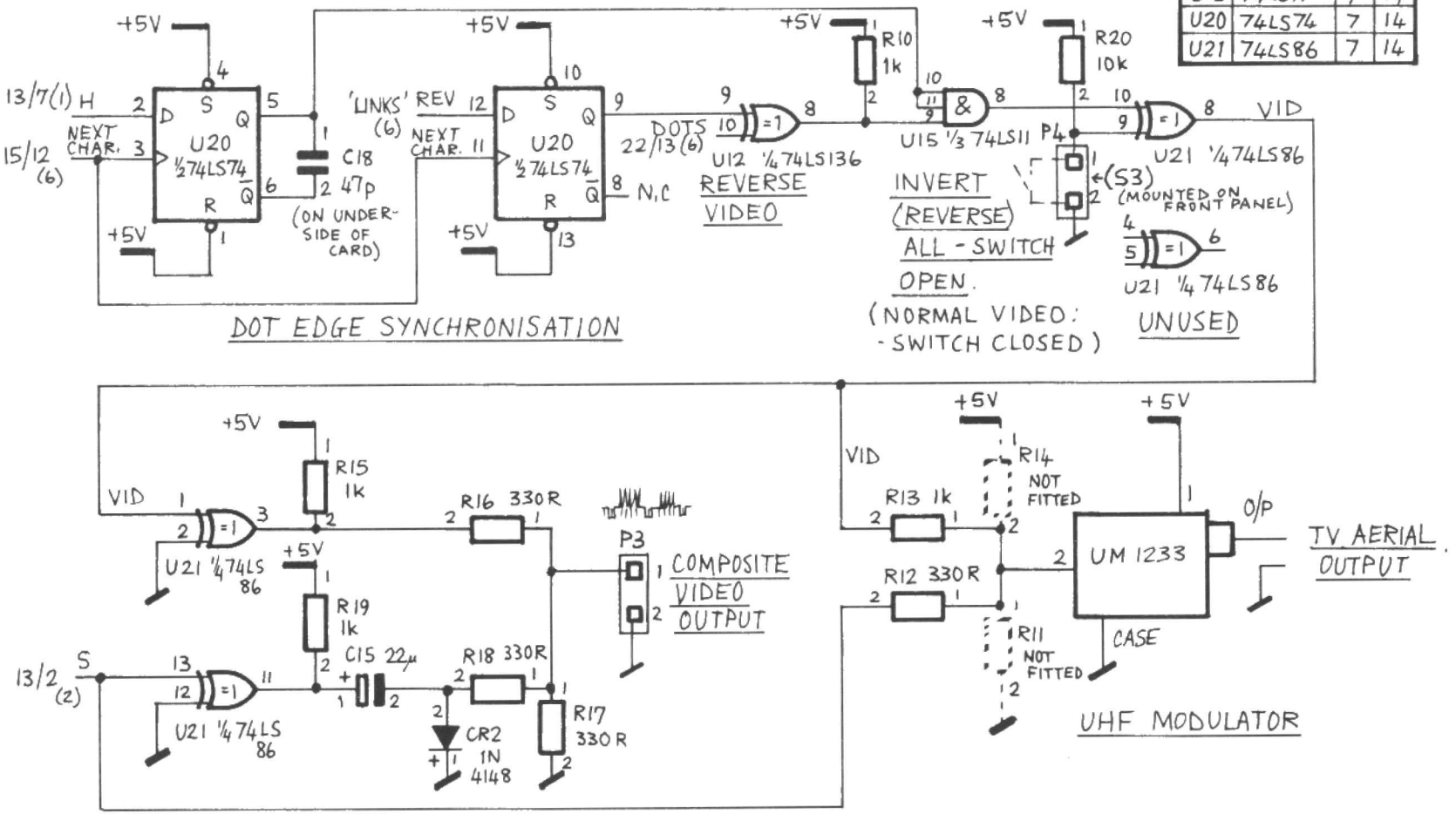
5 OF 8



IC No	TYPE	0V	+5V
U4	74LS14	7	14
U15	74LS11	7	14
U22	74LS166	8	16
U23	2716-CG2	12	24
U24	2716-CG1	12	24

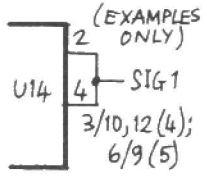
	Drawn D.M.P	Interak
	Date 9.11.82	VDU-K CIRCUIT DIAGRAM, SHEET 6: CHARACTOR GENERATOR(S), AND DOT RATE SHIFT REGISTER
	Scale –	6 OF 8

IC NO	TYPE	0V	+5V
U12	74LS136	7	14
U15	74LS11	7	14
U20	74LS74	7	14
U21	74LS86	7	14

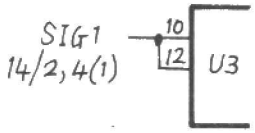


Drawn	D.M.P	Interak
Date	9.11.82	VDU-K CIRCUIT DIAGRAM, SHEET 7: SYNCHRONISATION, AND UHF MODULATOR
Scale	–	7 OF 8

KEY TO SYMBOLS USED ON CIRCUIT DIAGRAMS



OUTPUT PINS 2 AND 4 OF U14 PRODUCE A SIGNAL CALLED SIG1, WHICH IS CONNECTED TO U3 PINS 10, 12 (SHEET 4); AND U6 PIN 9 (SHEET 5).



INPUT PINS 10 AND 12 OF U3 RECEIVE A SIGNAL CALLED SIG1 WHOSE SOURCE IS U14 PINS 2,4 (SHEET 1).

0·1" PITCH EDGE CONNECTOR POSITION EG. A2 IS SIDE A, PIN 2; B3 IS SIDE B PIN 3, ETC. BUS SIGNAL NAME.

CONNECTION PAD OR PIN.

POSITION WHERE TRACK MAY BE CUT FOR SOME SPECIAL PURPOSE; ALTERNATIVE CONNECTION SHOWN DOTTED.

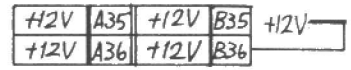
WIRE LINK (EG. WIRE WRAPPED TO TERMINAL PINS) SHOWN SOLID. ALTERNATIVE POSITION SHOWN DOTTED.

0V, EARTH CONNECTION.

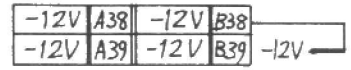
CONNECTION TO NAMED POWER SUPPLY RAIL.

POWER SUPPLIES

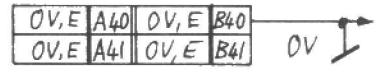
(EDGE CONNECTOR PINS A37, B37 REMOVED FOR POLARISING KEY)



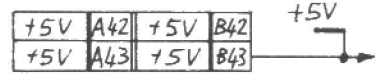
+12V NOT USED ON THIS CARD.



-12V NOT USED ON THIS CARD.



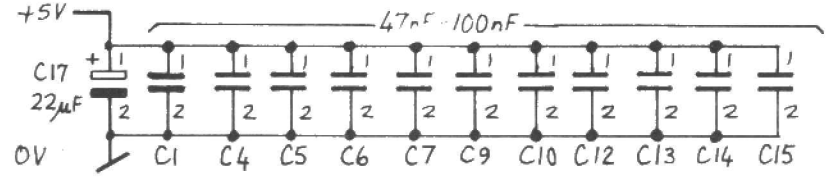
0V, EARTH POWER RAIL.



+5V POWER RAIL.

IC POWER SUPPLY CONNECTIONS ARE LISTED IN A TABLE IN ONE CORNER OF EACH SHEET OF THE MAIN CIRCUIT DIAGRAMS. FOR CLARITY OF LOGIC FLOW THE POWER SUPPLY CONNECTIONS ARE NOT NORMALLY INCLUDED ON THE GRAPHIC PART OF THE CIRCUIT DIAGRAMS. CONNECTIONS TO THE POWER SUPPLY RAILS FOR OTHER PURPOSES (E.G. ENABLES, DISABLES ETC.) ARE SHOWN.

DECOUPLING CAPACITORS

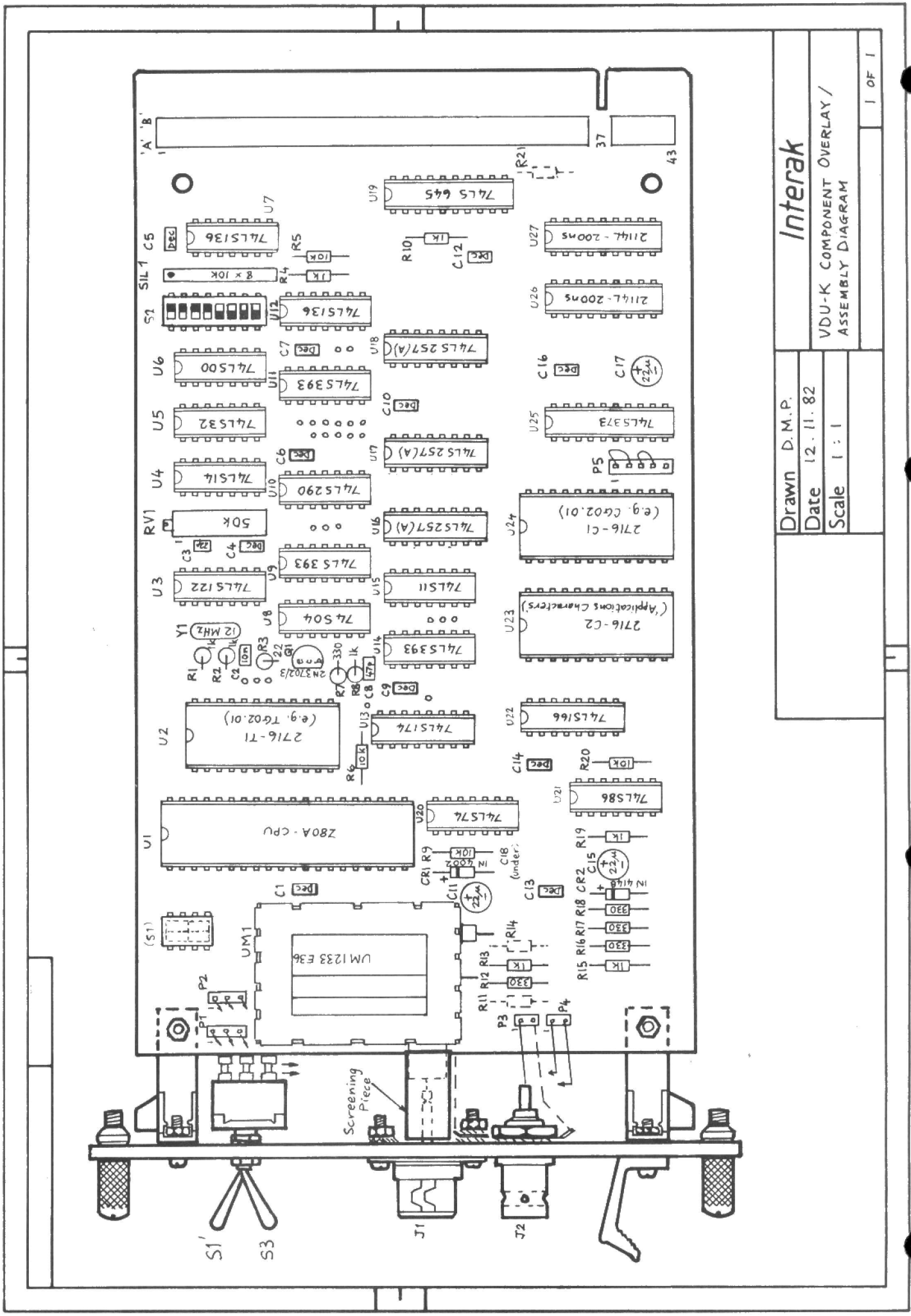


Drawn	D.M.P.
Date	9.11.82
Scale	-

Interak

VDU-K CIRCUIT DIAGRAM, SHEET 8: KEY TO SYMBOLS, AND POWER SUPPLIES

8 OF 8


Interak
VDU-K COMPONENT OVERLAY / ASSEMBLY DIAGRAM
1 OF 1
Drawn D.M.P.
Date 12.11.82
Scale 1:1
'A' 'B'
1
37
43
74LS 645
U19
R21
74LS136
U7
C5
SIL 1
8 x 10K
R4
R5
10K
1K
R10
C12
2114 - 200ns
U27
U26
S2
74LS136
U12
74LS 257(A)
U18
C7
74LS00
U6
74LS393
U11
C10
74LS32
U5
74LS 257(A)
U17
C6
74LS14
U4
74LS290
U10
C16
C17
22µ
74LS373
U25
P5
RV1
50K
74LS 257(A)
U16
2716 - C1 (e.g. C6O2.01)
U24
C3
C4
74LS 393
U9
74LS122
U3
74LS11
U15
74LS 04
U8
Y1
12 MHz
74LS393
U14
2716 - C2 ('Application Characters')
U23
R1
R2
R3
2N3702/3
330
1k
R7
R8
C8
C9
74LS166
U22
2716 - T1 (e.g. T6O2.01)
U2
74LS174
U13
R6
C14
R20
74LS86
U21
Z80A - CPU
U1
74LS74
U20
R19
CR1
R9
C18 (under)
C15
CR2
C11
C13
C1
R14
R13
R12
R11
330
R15 R16 R17 R18
(S1)
UM1
UM 1233 E36
P2
P1
P3
P4
Screening Piece
S1
S3
J1
J2

COMPONENT PARTS LIST FOR VDU-K CARD

Issue 3 Date: November 1982

LISTED BY COMPONENT REFERENCE NUMBER

PCB
*1 off PCB VDU-K

Resistors 0.25W (0.1" & 0.5" pitch)

R1	1k	0.1"	R12	330R	0.5"
R2	1k	0.1"	R13	1k	0.5"
R3	22R	0.1"	*R14	-	0.5"
R4	1k	0.5"	R15	1k	0.5"
R5	10k	0.5"	R16	330R	0.5"
R6	10k	0.5"	R17	330R	0.5"
R7	330R	0.1"	R18	330R	0.5"
R8	1k	0.1"	R19	1k	0.5"
R9	10k	0.5"	R20	10k	0.5"
R10	1k	0.5"	*R21	-	0.5
*R11	-	0.5"	("-" = not used)		

SIL Resistor (Use Socket)
SIL1 9-pin 8x10k

Variable Resistor (Multiturn Type)
RV1 50k

Capacitors

C1	Dec		0.2"	C10	Dec		0.2"
C2	10n	Cer	0.1"	C11	22µ	Al	0.2"
C3	22p	Cer	0.1"	C12	Dec		0.2"
C4	Dec		0.2"	C13	Dec		0.2"
C5	Dec		0.2"	C14	Dec		0.2"
C6	Dec		0.2"	C15	22µ	Al	0.2"
C7	Dec		0.2"	C16	Dec		0.2"
C8	47p	Cer	0.1"	C17	22µ	Al	0.2"
C9	Dec		0.2"	C18	47p	Cer	0.1"
(C3 has 5% tol)				(C18 mounted under)			

"Dec" = 47n-100n Decoupling grade polyester, or Ceramic

Diodes

CR1	1N4002	0.5"	CR2	1N4148	0.5"

Transistor
Q1 2N3702/3 (PNP)

Quartz Crystal
Y1 12.0 MHz

LISTED BY COMPONENT VALUE

PCB
*1 off PCB VDU-K

Resistors 0.25W

22R	1	R3
330R	5	R7,12,16-18
1k	8	R1,2,4,8,10,13,15,19
10k	4	R5,6,9,20
-	3	*R11,14,21

SIL Resistor (Use Socket) 
SIL1 9-pin 8x10k

Variable Resistor (Multiturn) 
50k 1 RV1

Capacitors 

22p	Cer	1	C3 (5% tolerance)
47p	Cer	2	C8,18 (18 under)
10n	Cer	1	C2
Dec		11	C1,4-7,9,10,12-14,15
22µ	Al	3	C11,15,17

"Cer" = Ceramic
"Dec" = 47n-100n Decoupling grade polyester, or Ceramic
"Al" = Low Leakage Min. Aluminium

Diodes

1N4002	1	CR1	a  k
1N4148	1	CR2	a  k

Transistor
2N3702/3 1 Q1 

Quartz Crystal 
Y1 12.0 MHz

COMPONENT PARTS LIST FOR VDU-K CARD (continued)

LISTED BY COMPONENT REFERENCE NUMBER

Integrated Circuits (Use Sockets)

U1	Z80A-CPU	(40)	U22	74LS166	(16)
U2	2716-TG	(24)	*U23	2716-C2	(24)
U3	74LS122	(14)	U24	2716-C1	(24)
U4	74LS14	(14)	U25	74LS373	(20)
U5	74LS32	(14)	U26	2114L-200	(18)
U6	74LS00	(14)	U27	2114L-200	(18)
U7	74LS136	(14)			
U8	74S04	(14)			
U9	74LS393	(14)			
U10	74LS290	(14)			
U11	74LS393	(14)			
U12	74LS136	(14)			
U13	74LS174	(16)			
U14	74LS393	(14)			
U15	74LS11	(14)			
U16	74LS257	(16)			
U17	74LS257	(16)			
U18	74LS257	(16)			
U19	74LS645	(20)			
U20	74LS74	(14)			
U21	74LS86	(14)			

0.1" Pitch Pin Assemblies

P1	3-pin	P4	2-pin
P2	3-pin	P5	5-pin
P3	2-pin		

UHF Modulator

*UM1 UM1233E36 Wide Bandwidth

Sundry

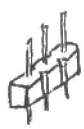
DIL Sockets, switches, other hardware
- see next page

LISTED BY COMPONENT VALUE

Integrated Circuits (Use Sockets)

2114L-200	2	U26,27
2716-C1	1	U24
*2716-C2	1	U23
2716-T1	1	U2
74LS00	1	U6
74LS11	1	U15
74LS14	1	U4
74LS32	1	U5
74LS74	1	U20
74LS86	1	U21
74LS122	1	U3
74LS136	2	U7,12
74LS166	1	U22
74LS174	1	U13
74LS257	3	U16-18
74LS290	1	U10
74LS373	1	U25
74LS393	3	U9,11,14
74LS645	1	U19
74S04	1	U8
Z80A-CPU	1	U1

0.1" Pitch Pin Assemblies.



2 pin	2	P3,P4
3 pin	2	P1,P2
5 pin	1	P5

UHF Modulator

*UM1233E36	1	UM1

Sundry

DIL Sockets, switches, other hardware
- see next page

COMPONENT PARTS LIST FOR VDU-K CARD (continued)

DIL & SIL Sockets

8-pin	1	S1	20-pin	2	U19,25
14-pin	14	U3-12,14,15,20,21	24-pin	3	U2,23,24
16-pin	6	S2; U13,16-18,22	40-pin	1	U1
18-pin	2	U26,27			

SIL Socket
9 pin 0.1" pitch socket strip (for SIL 1)

Sundry

Pre-stripped Insulated Wire (Including some spares)
5 off 25mm (for links)

Silicone Rubber Sleeving (Including spare)
2 off 20mm x 1.5mm dia. precut (UHF Modulator output insulation)

Tinned copper wire 24 swg (for connecting J1) 75mm

1 off Solder Tag (for connecting J1)

Extension Screening Piece for UHF Output
*1 off 18mm long x 10mm dia.

Switches
*S1' Front Panel mounted Min. Toggle DPDT (or *S1 8-pin DPDT DIL switch)
*S2 16-pin 8xSPST
*S3 Front Panel mounted Min. Toggle SPST

*1 off Coaxial TV Aerial Connector J1
*1 off BNC Video Connector and 0V Tag J2

Card Front
*1 off Kit (1 inch wide) including fixings and mounting brackets; new type or old (RS) type, according to type of rack used.

M2.5 Fixings. (Generally Steel, Supadriv)
*2 off Screws 10mm Panhead (For fixing J1 to card front)
*3 off Serrated Washers.
*2 off Nuts.

Note Options: The items marked "" in the parts lists are not supplied in the standard kit of parts for the VDU-K; they are however all available separately, as indeed are all the components, including for example the timing generator and character generator EPROMs.

Resistor Colour Code (Ignore last band (generally gold))
22R Red, Red, Black
330R Orange, Orange, Brown
1k Brown, Black, Red
10k Brown, Black, Orange